

ZQA SOLE UMA SYSTEM DIAGRAM

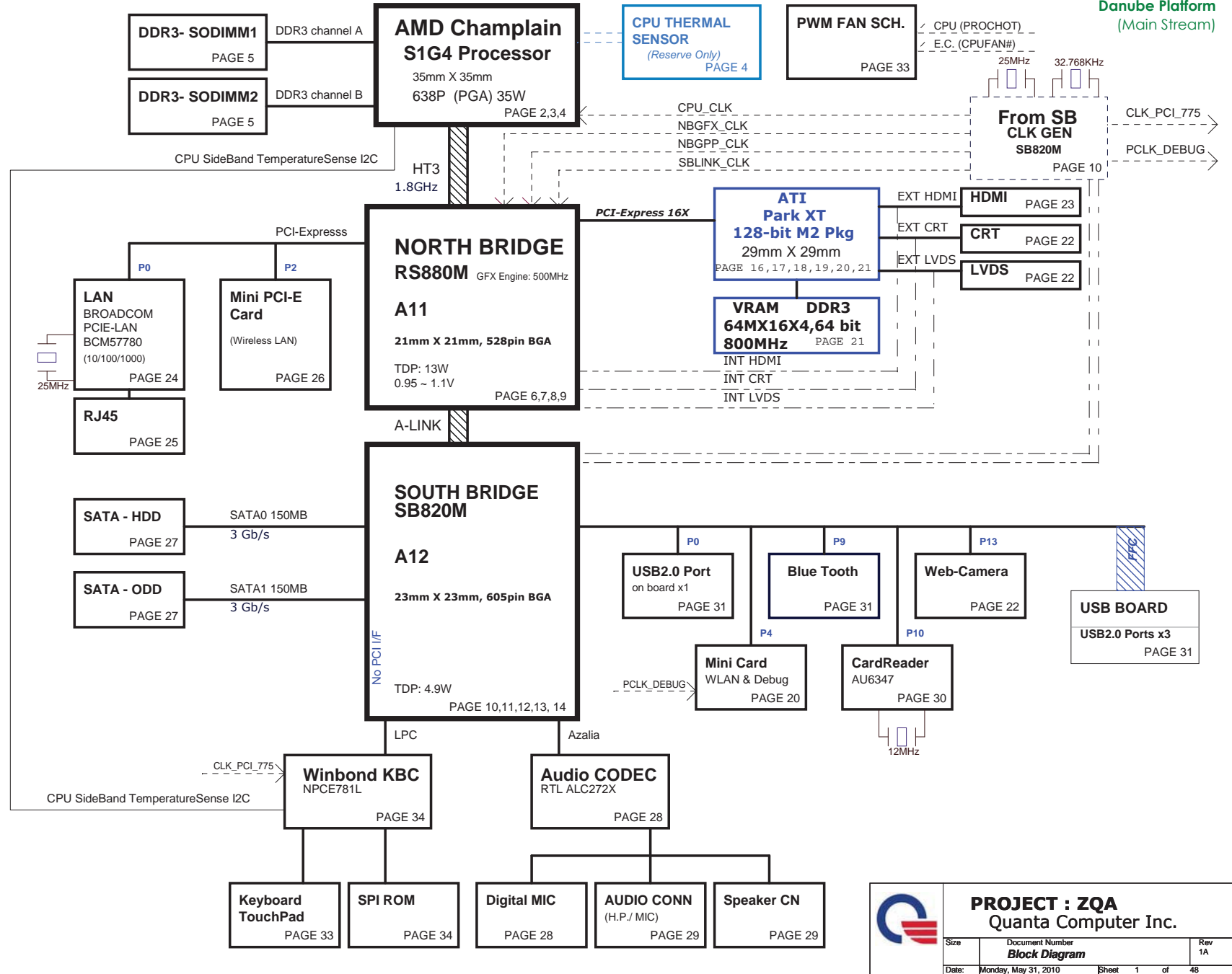


Danube Platform
(Main Stream)

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

IV@ -----> iGPU EV@ -----> dGPU
SPE@ -----> Option Notice



CHARGER (ISL88731A) PAGE 35

AMD CPU CORE (ISL6265) PAGE 37

NB_CORE (UP6111AQDD) PAGE 39

0.9V/DDR 1.5V(RT8207) PAGE 40

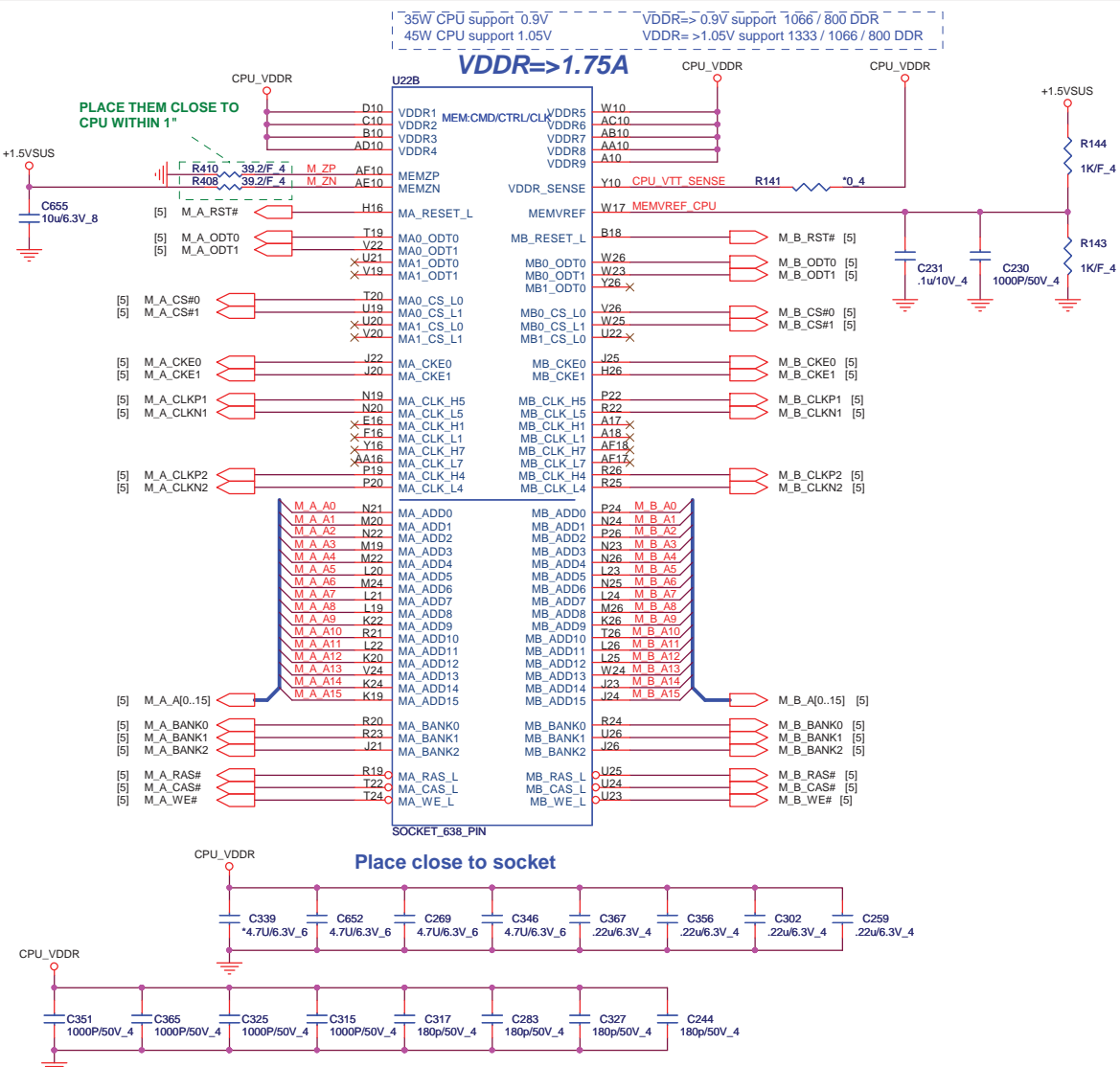
SYSTEM 5V/3V (RT8206) PAGE 36

1.1V(UP6111AQDD) PAGE 38

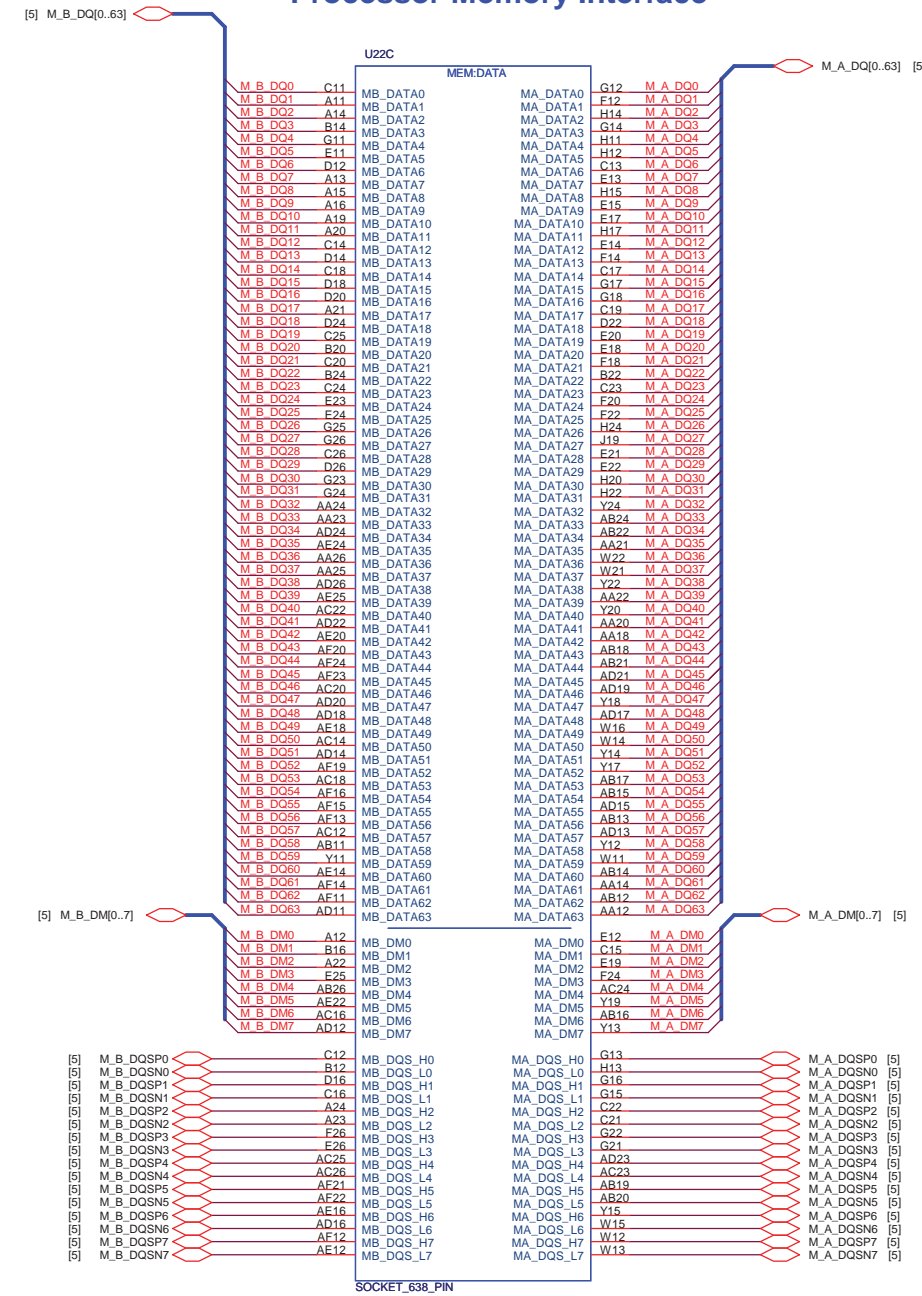
Discharge /Thermal protec PAGE 44

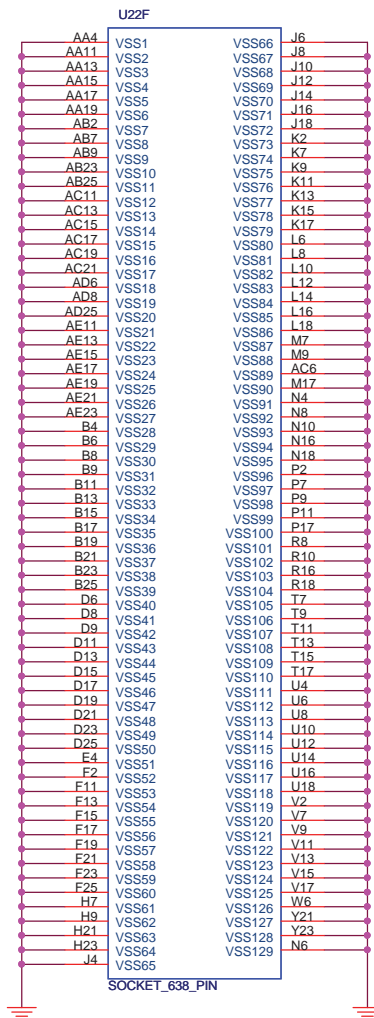
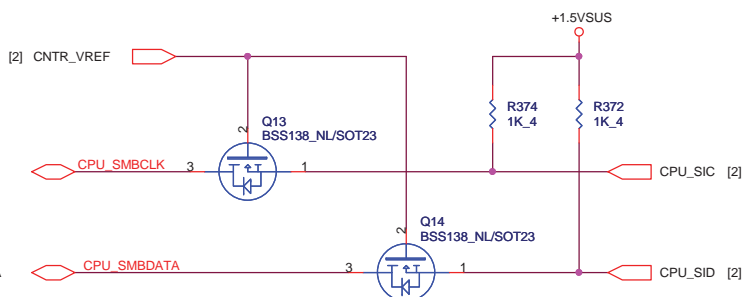
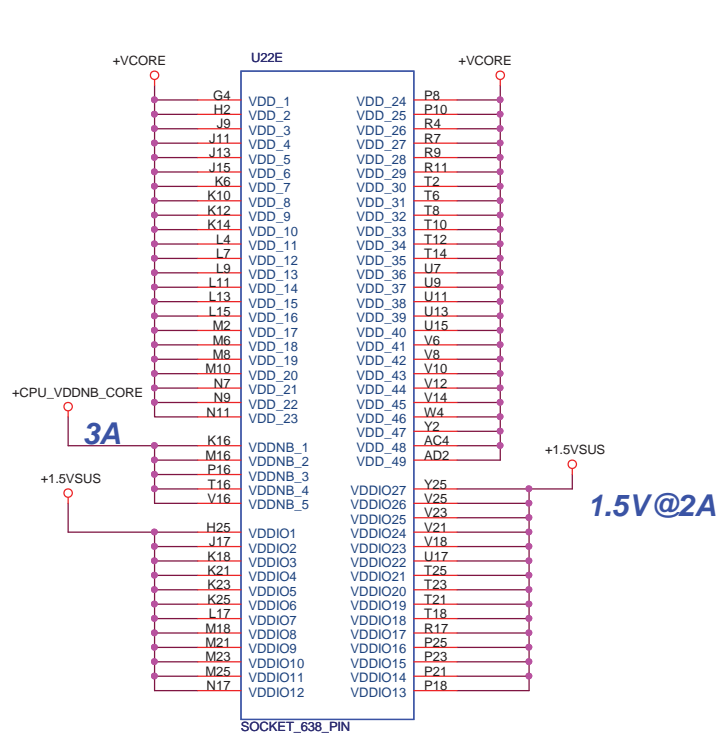
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
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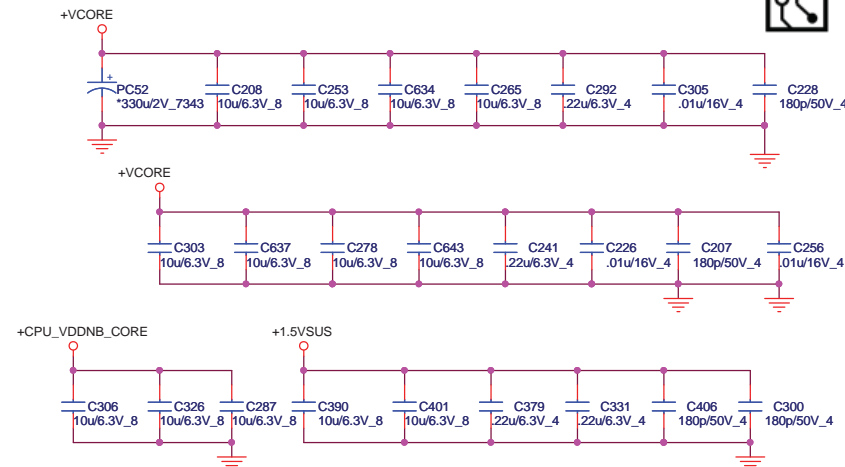


Processor Memory Interface

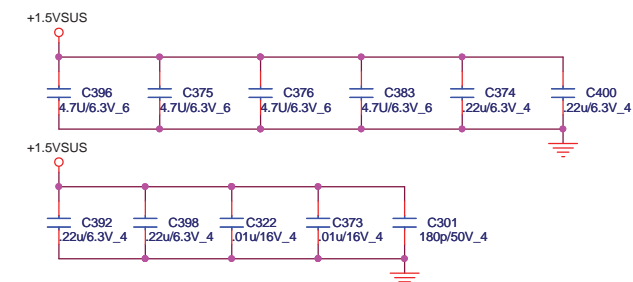




BOTTOM SIDE DECOUPLING

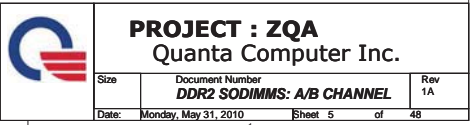


DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND





U16A		PART 1 OF 6		HYPER TRANSPORT CPU I/F	
[2] HT_CADOUTP0	HT_CADOUTP0 Y25	HT_RXCAD0P	HT_TXCAD0P D24	HT_CADINP0	HT_CADINP0 [2]
[2] HT_CADOUTN0	HT_CADOUTN0 Y24	HT_RXCAD0N	HT_TXCAD0N D25	HT_CADINN0	HT_CADINN0 [2]
[2] HT_CADOUTP1	HT_CADOUTP1 Y23	HT_RXCAD1P	HT_TXCAD1P D26	HT_CADINP1	HT_CADINP1 [2]
[2] HT_CADOUTN1	HT_CADOUTN1 Y22	HT_RXCAD1N	HT_TXCAD1N D27	HT_CADINN1	HT_CADINN1 [2]
[2] HT_CADOUTP2	HT_CADOUTP2 Y25	HT_RXCAD2P	HT_TXCAD2P E24	HT_CADINP2	HT_CADINP2 [2]
[2] HT_CADOUTN2	HT_CADOUTN2 Y24	HT_RXCAD2N	HT_TXCAD2N E25	HT_CADINN2	HT_CADINN2 [2]
[2] HT_CADOUTP3	HT_CADOUTP3 U24	HT_RXCAD3P	HT_TXCAD3P E26	HT_CADINP3	HT_CADINP3 [2]
[2] HT_CADOUTN3	HT_CADOUTN3 U25	HT_RXCAD3N	HT_TXCAD3N E22	HT_CADINN3	HT_CADINN3 [2]
[2] HT_CADOUTP4	HT_CADOUTP4 T25	HT_RXCAD4P	HT_TXCAD4P H22	HT_CADINP4	HT_CADINP4 [2]
[2] HT_CADOUTN4	HT_CADOUTN4 T24	HT_RXCAD4N	HT_TXCAD4N H23	HT_CADINN4	HT_CADINN4 [2]
[2] HT_CADOUTP5	HT_CADOUTP5 P22	HT_RXCAD5P	J25 HT_CADINP5	HT_CADINP5	HT_CADINP5 [2]
[2] HT_CADOUTN5	HT_CADOUTN5 P23	HT_RXCAD5N	J24 HT_CADINN5	HT_CADINN5	HT_CADINN5 [2]
[2] HT_CADOUTP6	HT_CADOUTP6 P25	HT_RXCAD6P	K24 HT_CADINP6	HT_CADINP6	HT_CADINP6 [2]
[2] HT_CADOUTN6	HT_CADOUTN6 P24	HT_RXCAD6N	K25 HT_CADINN6	HT_CADINN6	HT_CADINN6 [2]
[2] HT_CADOUTP7	HT_CADOUTP7 N24	HT_RXCAD7P	K23 HT_CADINP7	HT_CADINP7	HT_CADINP7 [2]
[2] HT_CADOUTN7	HT_CADOUTN7 N25	HT_RXCAD7N	K22 HT_CADINN7	HT_CADINN7	HT_CADINN7 [2]
[2] HT_CADOUTP8	HT_CADOUTP8 AC24	HT_RXCAD8P	E21 HT_CADINP8	HT_CADINP8	HT_CADINP8 [2]
[2] HT_CADOUTN8	HT_CADOUTN8 AC25	HT_RXCAD8N	G21 HT_CADINN8	HT_CADINN8	HT_CADINN8 [2]
[2] HT_CADOUTP9	HT_CADOUTP9 AB25	HT_RXCAD9P	G20 HT_CADINP9	HT_CADINP9	HT_CADINP9 [2]
[2] HT_CADOUTN9	HT_CADOUTN9 AB24	HT_RXCAD9N	H21 HT_CADINN9	HT_CADINN9	HT_CADINN9 [2]
[2] HT_CADOUTP10	HT_CADOUTP10 AA24	HT_RXCAD10P	H20 HT_CADINP10	HT_CADINP10	HT_CADINP10 [2]
[2] HT_CADOUTN10	HT_CADOUTN10 AA25	HT_RXCAD10N	J21 HT_CADINN10	HT_CADINN10	HT_CADINN10 [2]
[2] HT_CADOUTP11	HT_CADOUTP11 Y22	HT_RXCAD11P	J18 HT_CADINP11	HT_CADINP11	HT_CADINP11 [2]
[2] HT_CADOUTN11	HT_CADOUTN11 Y21	HT_RXCAD11N	K17 HT_CADINN11	HT_CADINN11	HT_CADINN11 [2]
[2] HT_CADOUTP12	HT_CADOUTP12 W21	HT_RXCAD12P	L19 HT_CADINP12	HT_CADINP12	HT_CADINP12 [2]
[2] HT_CADOUTN12	HT_CADOUTN12 W20	HT_RXCAD12N	L19 HT_CADINN12	HT_CADINN12	HT_CADINN12 [2]
[2] HT_CADOUTP13	HT_CADOUTP13 V20	HT_RXCAD13P	M19 HT_CADINP13	HT_CADINP13	HT_CADINP13 [2]
[2] HT_CADOUTN13	HT_CADOUTN13 V21	HT_RXCAD13N	L18 HT_CADINN13	HT_CADINN13	HT_CADINN13 [2]
[2] HT_CADOUTP14	HT_CADOUTP14 U20	HT_RXCAD14P	M21 HT_CADINP14	HT_CADINP14	HT_CADINP14 [2]
[2] HT_CADOUTN14	HT_CADOUTN14 U21	HT_RXCAD14N	P21 HT_CADINN14	HT_CADINN14	HT_CADINN14 [2]
[2] HT_CADOUTP15	HT_CADOUTP15 U19	HT_RXCAD15P	P18 HT_CADINP15	HT_CADINP15	HT_CADINP15 [2]
[2] HT_CADOUTN15	HT_CADOUTN15 U18	HT_RXCAD15N	M18 HT_CADINN15	HT_CADINN15	HT_CADINN15 [2]
[2] HT_CLKOUTP0	HT_CLKOUTP0 T22	HT_RXCLK0P	H24 HT_CLKINP0	HT_CLKINP0	HT_CLKINP0 [2]
[2] HT_CLKOUTN0	HT_CLKOUTN0 T23	HT_RXCLK0N	H25 HT_CLKINN0	HT_CLKINN0	HT_CLKINN0 [2]
[2] HT_CLKOUTP1	HT_CLKOUTP1 AB23	HT_RXCLK1P	L21 HT_CLKINP1	HT_CLKINP1	HT_CLKINP1 [2]
[2] HT_CLKOUTN1	HT_CLKOUTN1 AA22	HT_RXCLK1N	L20 HT_CLKINN1	HT_CLKINN1	HT_CLKINN1 [2]
[2] HT_CTLOUTP0	HT_CTLOUTP0 M22	HT_RXTCL0P	M24 HT_CTLINP0	HT_CTLINP0	HT_CTLINP0 [2]
[2] HT_CTLOUTN0	HT_CTLOUTN0 M23	HT_RXTCL0N	M25 HT_CTLINN0	HT_CTLINN0	HT_CTLINN0 [2]
[2] HT_CTLOUTP1	HT_CTLOUTP1 R21	HT_RXTCL1P	P19 HT_CTLINP1	HT_CTLINP1	HT_CTLINP1 [2]
[2] HT_CTLOUTN1	HT_CTLOUTN1 R20	HT_RXTCL1N	P18 HT_CTLINN1	HT_CTLINN1	HT_CTLINN1 [2]
R349	30T/F 4	HT_RXCALP C23	HT_TXCALP B24	R350	30T/F 4
	HT_RXCALN A24	HT_RXCALP HT_RXCALN	HT_TXCALP HT_TXCALN		

Pin Configuration Diagram for RS880/RX881

Top Section (Pins 1-16):

- Pin 1: ~~AB12~~ MEM_A0(NC)
- Pin 2: ~~AE16~~ MEM_A1(NC)
- Pin 3: ~~V11~~ MEM_A2(NC)
- Pin 4: ~~AE15~~ MEM_A3(NC)
- Pin 5: ~~AD14~~ MEM_A4(NC)
- Pin 6: ~~AE15~~ MEM_A5(NC)
- Pin 7: ~~AD14~~ MEM_A6(NC)
- Pin 8: ~~AD13~~ MEM_A7(NC)
- Pin 9: ~~AD15~~ MEM_A8(NC)
- Pin 10: ~~AC18~~ MEM_A9(NC)
- Pin 11: ~~AE13~~ MEM_A11(NC)
- Pin 12: ~~AC14~~ MEM_A12(NC)
- Pin 13: ~~Y14~~ MEM_A13(NC)
- Pin 14: ~~AD16~~ MEM_BA0(NC)
- Pin 15: ~~AE17~~ MEM_BA1(NC)
- Pin 16: ~~AD17~~ MEM_BA2(NC)

Bottom Section (Pins 17-26):

- Pin 17: ~~W12~~ MEM_RASB(NC)
- Pin 18: ~~Y12~~ MEM_CASB(NC)
- Pin 19: ~~AD18~~ MEM_WEB(NC)
- Pin 20: ~~AB13~~ MEM_CSb(NC)
- Pin 21: ~~AB18~~ MEM_CKE(NC)
- Pin 22: ~~Y14~~ MEM_ODT(NC)
- Pin 23: ~~Y15~~ MEM_CKP(NC)
- Pin 24: ~~W14~~ MEM_CKN(NC)
- Pin 25: ~~AE12~~ MEM_COMPp(NC)
- Pin 26: ~~AD12~~ MEM_COMPn(NC)

Internal Connections and Power Rails:

- MEM_A0(NC) to MEM_A13(NC):** Connected to MEM_DQ0/DVO_VSYNC(NC) and MEM_DQ1/DVO_HSYNC(NC).
- MEM_A11(NC) to MEM_A13(NC):** Connected to MEM_DQ2/DVO_DE(NC) and MEM_DQ3/DVO_D0(NC).
- MEM_A4(NC) to MEM_A13(NC):** Connected to MEM_DQ4(NC) and MEM_DQ5/DVO_D1(NC).
- MEM_A6(NC) to MEM_A13(NC):** Connected to MEM_DQ6/DVO_D2(NC) and MEM_DQ7/DVO_D4(NC).
- MEM_A8(NC) to MEM_A13(NC):** Connected to MEM_DQ8/DVO_D3(NC) and MEM_DQ9/DVO_D5(NC).
- MEM_A11(NC) to MEM_A13(NC):** Connected to MEM_DQ10/DVO_D6(NC) and MEM_DQ11/DVO_D7(NC).
- MEM_A12(NC) to MEM_A13(NC):** Connected to MEM_DQ12(NC) and MEM_DQ13/DVO_D9(NC).
- MEM_BA0(NC) to MEM_BA2(NC):** Connected to MEM_DQ14/DVO_D10(NC) and MEM_DQ15/DVO_D11(NC).
- MEM_RASB(NC) to MEM_CASB(NC):** Connected to MEM_DQS0P/DVO_IDCKP(NC) and MEM_DQS0N/DVO_IDCKN(NC).
- MEM_WEB(NC) to MEM_CSb(NC):** Connected to MEM_DQS1P(NC) and MEM_DQS1N(NC).
- MEM_CKE(NC) to MEM_ODT(NC):** Connected to MEM_DM0(NC) and MEM_DM1/DVO_D8(NC).
- MEM_CKP(NC) to MEM_CKN(NC):** Connected to IOPLLVD18(NC) and IOPLLVD1(NC).
- MEM_COMPp(NC) to MEM_COMPn(NC):** Connected to IOPLLVS(NC) and MEM_VREF(NC).

Power Connections:

- 1.8V:** Connected to AE23 and AE24.
- 1.1V:** Connected to AE23 and AE24.
- 15mA:** Connected to AD23.
- 26mA:** Connected to AE18.

[15] PEG_RXP[15..0] ← PEG_RXP[15..0]
[15] PEG_RXN[15..0] ← PEG_RXN[15..0]

[15] PEG_TXP[15..0] ← PEG_TXP[15..0]
[15] PEG_TXN[15..0] ← PEG_TXN[15..0]

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

U16B
PEG_RXP15 D4
PEG_RXN15 C4
PEG_RXP14 A3
PEG_RXN14 B3
PEG_RXP13 C2
PEG_RXN13 C1
PEG_RXP12 E5
PEG_RXN12 F5
PEG_RXP11 G5
PEG_RXN11 G6
PEG_RXP10 H5
PEG_RXN10 H6
PEG_RXP9 J6
PEG_RXN9 J5
PEG_RXP8 J7
PEG_RXN8 J8
PEG_RXP7 L5
PEG_RXN7 L6
PEG_RXP6 M8
PEG_RXN6 L8
PEG_RXP5 P7
PEG_RXN5 M7
PEG_RXP4 P5
PEG_RXN4 M5
PEG_RXP3 R8
PEG_RXN3 P8
PEG_RXP2 R6
PEG_RXN2 R5
PEG_RXP1 P4
PEG_RXN1 P3
PEG_RXP0 T4
PEG_RXN0 T3

PART 2 OF 6

PCIE I/F GFX

GFX_RX0P
GFX_RX0N
GFX_RX1P
GFX_RX1N
GFX_RX2P
GFX_RX2N
GFX_RX3P
GFX_RX3N
GFX_RX4P
GFX_RX4N
GFX_RX5P
GFX_RX5N
GFX_RX6P
GFX_RX6N
GFX_RX7P
GFX_RX7N
GFX_RX8P
GFX_RX8N
GFX_RX9P
GFX_RX9N
GFX_RX10P
GFX_RX10N
GFX_RX11P
GFX_RX11N
GFX_RX12P
GFX_RX12N
GFX_RX13P
GFX_RX13N
GFX_RX14P
GFX_RX14N
GFX_RX15P
GFX_RX15N

A5 PEG_TXP15 C C568
B5 PEG_TXN15 C C570
A4 PEG_TXP14 C C561
B4 PEG_TXN14 C C562
C3 PEG_TXP13 C C557
B2 PEG_TXN13 C C559
D1 PEG_TXP12 C C553
D2 PEG_TXN12 C C556
E2 PEG_TXP11 C C549
F1 PEG_TXN11 C C552
F4 PEG_TXP10 C C541
E3 PEG_TXN10 C C548
F1 PEG_TXP9 C C537
F2 PEG_TXN9 C C540
H4 PEG_TXP8 C C527
H3 PEG_TXN8 C C536
H1 PEG_TXP7 C C535
H2 PEG_TXN7 C C539
J2 PEG_TXP6 C C518
J1 PEG_TXN6 C C525
K4 PEG_TXP5 C C523
K3 PEG_TXN5 C C526
K1 PEG_TXP4 C C530
K2 PEG_TXN4 C C529
M4 PEG_TXP3 C C522
M3 PEG_TXN3 C C521
M1 PEG_TXP2 C C532
M2 PEG_TXN2 C C531
N2 PEG_TXP1 C C520
N1 PEG_TXN1 C C519
P1 PEG_TXP0 C C534
P2 PEG_TXN0 C C533

EV@.1u/10V_4 PEG_TXP15
EV@.1u/10V_4 PEG_TXN15
EV@.1u/10V_4 PEG_TXP14
EV@.1u/10V_4 PEG_TXN14
EV@.1u/10V_4 PEG_TXP13
EV@.1u/10V_4 PEG_TXN13
EV@.1u/10V_4 PEG_TXP12
EV@.1u/10V_4 PEG_TXN12
EV@.1u/10V_4 PEG_TXP11
EV@.1u/10V_4 PEG_TXN11
EV@.1u/10V_4 PEG_TXP10
EV@.1u/10V_4 PEG_TXN10
EV@.1u/10V_4 PEG_TXP9
EV@.1u/10V_4 PEG_TXN9
EV@.1u/10V_4 PEG_TXP8
EV@.1u/10V_4 PEG_TXN8
EV@.1u/10V_4 PEG_TXP7
EV@.1u/10V_4 PEG_TXN7
EV@.1u/10V_4 PEG_TXP6
EV@.1u/10V_4 PEG_TXN6
EV@.1u/10V_4 PEG_TXP5
EV@.1u/10V_4 PEG_TXN5
EV@.1u/10V_4 PEG_TXP4
EV@.1u/10V_4 PEG_TXN4
EV@.1u/10V_4 PEG_TXP3
EV@.1u/10V_4 PEG_TXN3
EV@.1u/10V_4 PEG_TXP2
EV@.1u/10V_4 PEG_TXN2
EV@.1u/10V_4 PEG_TXP1
EV@.1u/10V_4 PEG_TXN1
EV@.1u/10V_4 PEG_TXP0
EV@.1u/10V_4 PEG_TXN0

[24] PCIE_RX1+
[24] PCIE_RX1-

AE3
AD4
AE2
AD3

[26] PCIE_RXP2
[26] PCIE_RXN2

AD1
AD2
V5
W6
U5
U6
U8
U7

PCIE I/F GPP

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
GPP_RX4P
GPP_RX4N
GPP_RX5P
GPP_RX5N

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_TX4P
GPP_TX4N
GPP_TX5P
GPP_TX5N

AC1 PCIE_TXP0 C C546
AC2 PCIE_TXN0 C C545

.1u/10V_4
.1u/10V_4

PCIE_TX1+ [24]
PCIE_TX1- [24]

AA2 PCIE_TXP2 C C543
AA1 PCIE_TXN2 C C544

.1u/10V_4
.1u/10V_4

PCIE_TXP2 [26]
PCIE_TXN2 [26]

[10] A_RXP0
[10] A_RXN0
[10] A_RXP1
[10] A_RXN1
[10] A_RXP2
[10] A_RXN2
[10] A_RXP3
[10] A_RXN3

AA8
Y8
AA7
Y7
AA5
AA6
W5
Y5

PCIE I/F SB

SB_RX0P
SB_RX0N
SB_RX1P
SB_RX1N
SB_RX2P
SB_RX2N
SB_RX3P
SB_RX3N

AD7 A_TXP0 C C573
AE7 A_TXN0 C C569
AE6 A_TXP1 C C560
AD6 A_TXN1 C C563
AB6 A_TXP2 C C555
AC6 A_TXN2 C C558
AD5 A_TXP3 C C547
AE5 A_TXN3 C C551

.1u/10V_4
.1u/10V_4
.1u/10V_4
.1u/10V_4
.1u/10V_4
.1u/10V_4
.1u/10V_4
.1u/10V_4

A_TXP0 [10]
A_TXN0 [10]
A_TXP1 [10]
A_TXN1 [10]
A_TXP2 [10]
A_TXN2 [10]
A_TXP3 [10]
A_TXN3 [10]

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AC8 NB_PCIECALRP R326
AB8 NB_PCIECALRN R330

1.27K/F 4
2K/F 4

+1.1V

LAN

WLAN

SB

INT HDMI

PEG_TXP15 C C76
PEG_TXN15 C C78
PEG_TXP14 C C73
PEG_TXN14 C C75
PEG_TXP13 C C68
PEG_TXN13 C C71
PEG_TXP12 C C64
PEG_TXN12 C C67

IV@.1u/10V_4
IV@.1u/10V_4
IV@.1u/10V_4
IV@.1u/10V_4
IV@.1u/10V_4
IV@.1u/10V_4
IV@.1u/10V_4
IV@.1u/10V_4

IV_TX2_HDMI+ [23]
IV_TX2_HDMI- [23]
IV_TX1_HDMI+ [23]
IV_TX1_HDMI- [23]
IV_TX0_HDMI+ [23]
IV_TX0_HDMI- [23]
IV_TXC_HDMI- [23]



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For Check list JTAG



For A11 version

(02/10) Don't need 49.9 ohm PD.



STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

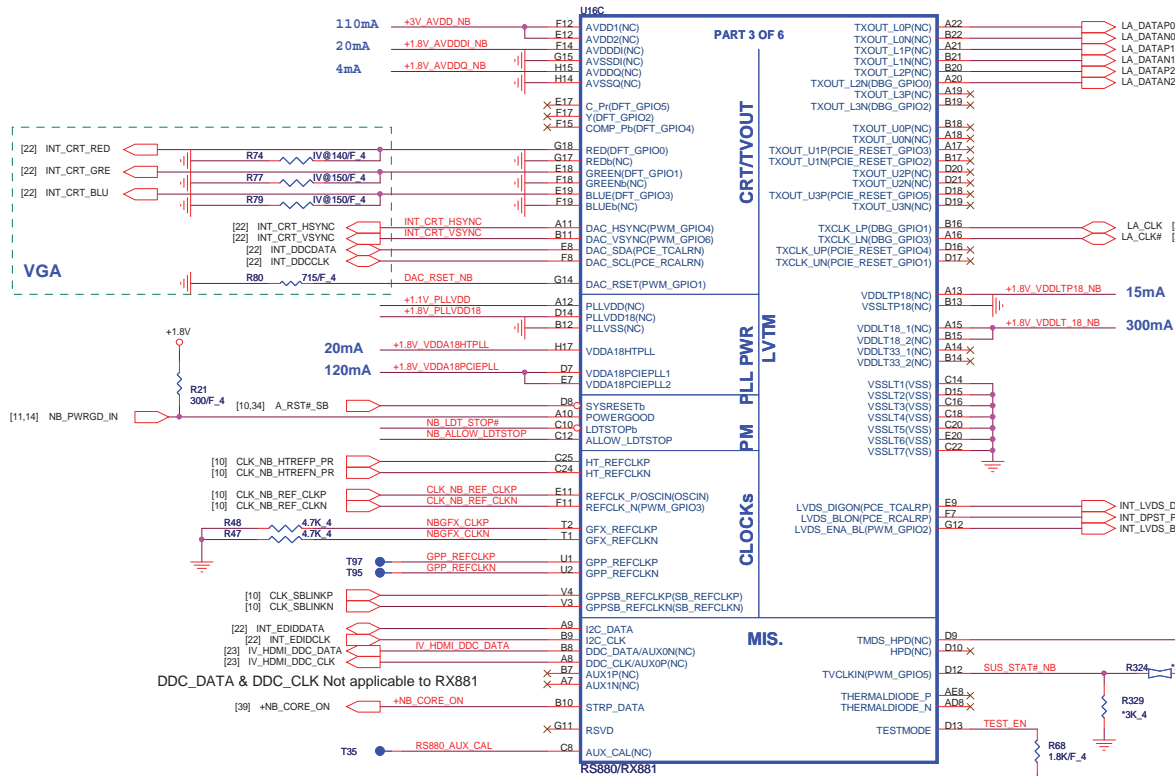


For external EEPROM Debug only

RS780/RX780/RS880



Display Port interface from PCIeGraphics (RS880/rs880M only)

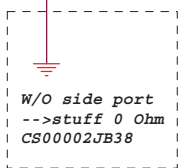


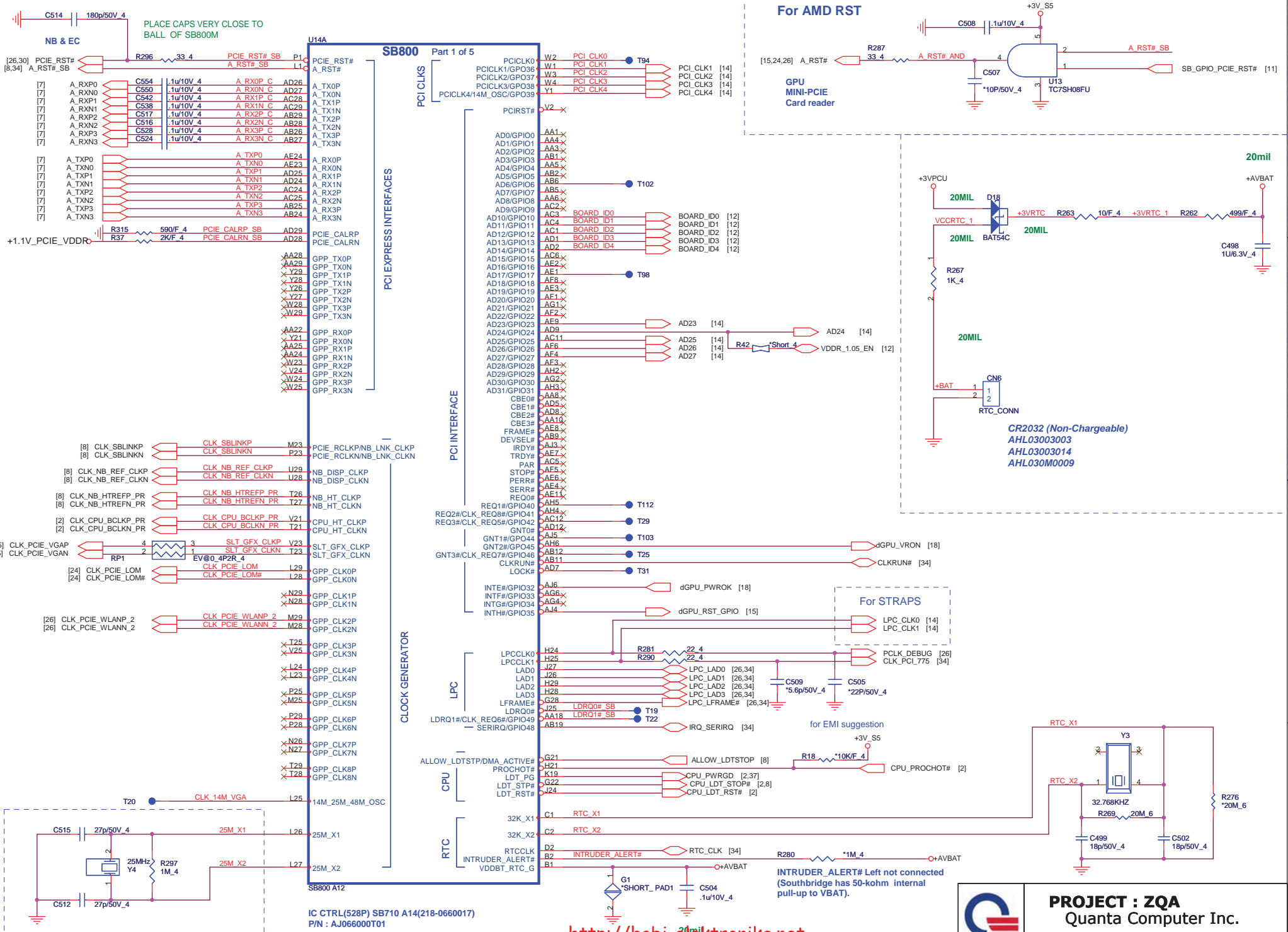
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NC only .Can't be install

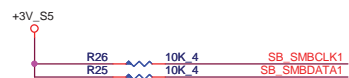


SCL0/SDATA0 is 3V tolerance. AMD datasheet define it

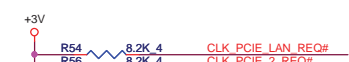
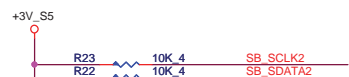
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer



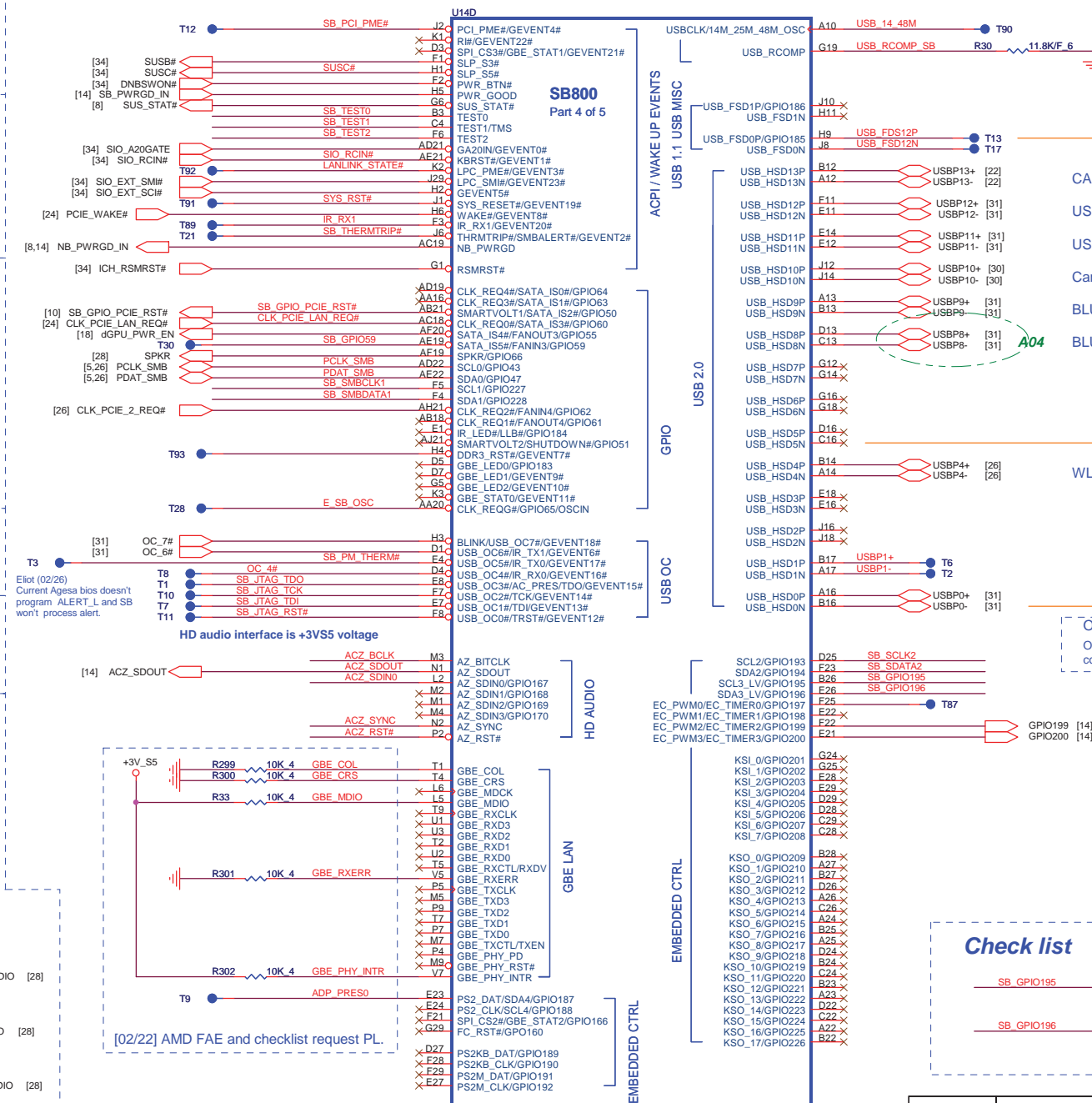
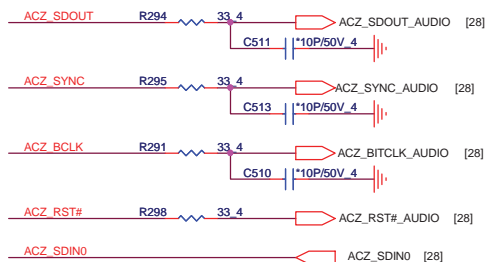
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it



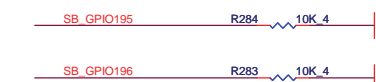
SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it



To Azalia



Check list



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number SB820-ACPI/GPIO/USB 2/4	Rev 1A
Date:	Monday, May 31, 2010	Sheet 11 of 48

Max trace length: 6"

SATA HDD

[27] SATA_TX0+
[27] SATA_TX0-

C567 |.01u/16V_4
C566 |.01u/16V_4

SATA_TX0+ C
SATA_TX0- C

AH9
AJ9

SATA_TX0P
SATA_TX0N

AH8
AJ8

SATA_RX0N
SATA_RX0P

AH10
AJ10

SATA_TX1P
SATA_TX1N

AG10
AF10

SATA_RX1N
SATA_RX1P

AG12
AF12

SATA_TX2P
SATA_TX2N

AJ12
AH12

SATA_RX2N
SATA_RX2P

AH14
AJ14

SATA_TX3P
SATA_TX3N

AG14
AF14

SATA_RX3N
SATA_RX3P

AG17
AF17

SATA_TX4P
SATA_TX4N

AJ17
AH17

SATA_RX4N
SATA_RX4P

SATA ODD

[27] SATA_TX1+
[27] SATA_TX1-

C565 |.01u/16V_4
C564 |.01u/16V_4

SATA_TX1+ C
SATA_TX1- C

AH10
AJ10

SATA_TX1P
SATA_TX1N

AG10
AF10

SATA_RX1N
SATA_RX1P

AG12
AF12

SATA_TX2P
SATA_TX2N

AJ12
AH12

SATA_RX2N
SATA_RX2P

AH14
AJ14

SATA_TX3P
SATA_TX3N

AG14
AF14

SATA_RX3N
SATA_RX3P

AG17
AF17

SATA_TX4P
SATA_TX4N

AJ17
AH17

SATA_RX4N
SATA_RX4P

AJ18
AH18

SATA_TX5P
SATA_TX5N

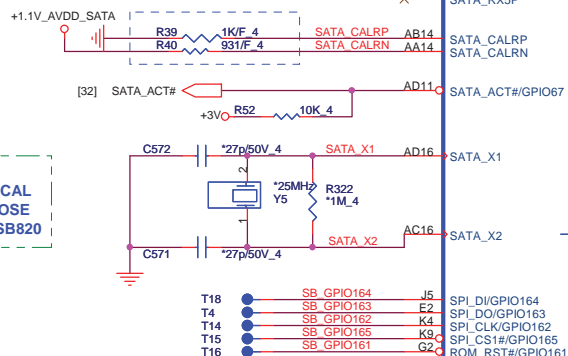
AH18
AJ18

SATA_RX5N
SATA_RX5P

SATA PORT 0,1,2,3 can support AHCI mode

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820



U14B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB800 A12

FC_CLK
FC_FBLKOUT
FC_FBLKIN
FC_OE#/GPIO145
FC_AVD#/GPIO146
FC_WE#/GPIO148
FC_CE1#/GPIO149
FC_CE2#/GPIO150
FC_INT1/GPIO144
FC_INT2/GPIO147
FC_ADQ0/GPIO128
FC_ADQ1/GPIO129
FC_ADQ2/GPIO130
FC_ADQ3/GPIO131
FC_ADQ4/GPIO132
FC_ADQ5/GPIO133
FC_ADQ6/GPIO134
FC_ADQ7/GPIO135
FC_ADQ8/GPIO136
FC_ADQ9/GPIO137
FC_ADQ10/GPIO138
FC_ADQ11/GPIO139
FC_ADQ12/GPIO140
FC_ADQ13/GPIO141
FC_ADQ14/GPIO142
FC_ADQ15/GPIO143

FANOUT0/GPIO52
FANOUT1/GPIO53
FANOUT2/GPIO54
FANIN0/GPIO56
FANIN1/GPIO57
FANIN2/GPIO58
TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174
TEMP_COMM
VIN0/GPIO175
VIN1/GPIO176
VIN2/GPIO177
VIN3/GPIO178
VIN4/GPIO179
VIN5/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182

NC1
NC2G27
Y2

BT_OFF#

WWAN_DET#

CPPE_NC1#

CRD_REQ1#

TEMPIN0

TEMPIN1

MB_THRMDA_SB

SB_GPIO174

TEMP_COMM

SB_GPIO175

SB_GPIO176

SIDE_PORT_ID0

SIDE_PORT_ID1

MEM_TVS

SB820_GPIO180

SB820_GPIO182

T88

T5

T27

T23

T24

T26

T104

T114

T115

T106

T107

T117

T118

T109

T108

T126

T116

T125

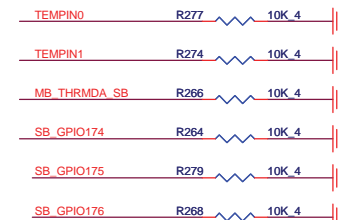
T124

T105

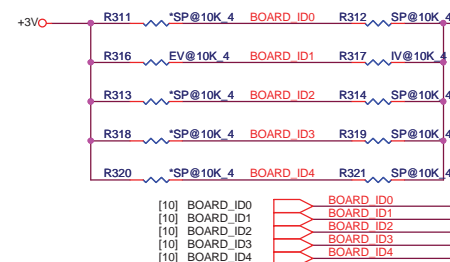
T123

IF THERE IS NO IDE, TEST POINTS FOR
DEBUG BUS IS MANDATORY

Check list

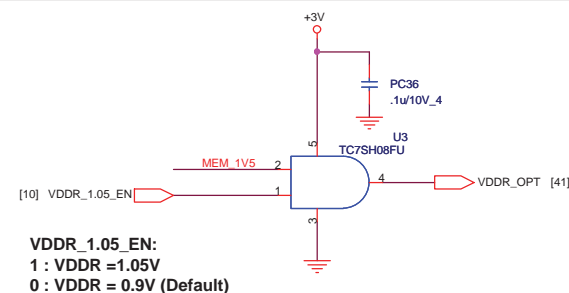


BOM check



	1	0
ID0		
ID1	DIS	UMA
ID2		
ID3		
ID4		

[10] BOARD_ID0
[10] BOARD_ID1
[10] BOARD_ID2
[10] BOARD_ID3
[10] BOARD_ID4



VDDR_1.05_EN:
1 : VDDR = 1.05V
0 : VDDR = 0.9V (Default)



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number SB820-SATA/IDE/SPI 3/4	Rev 1A
Date:	Monday, May 31, 2010	Sheet 12 of 48

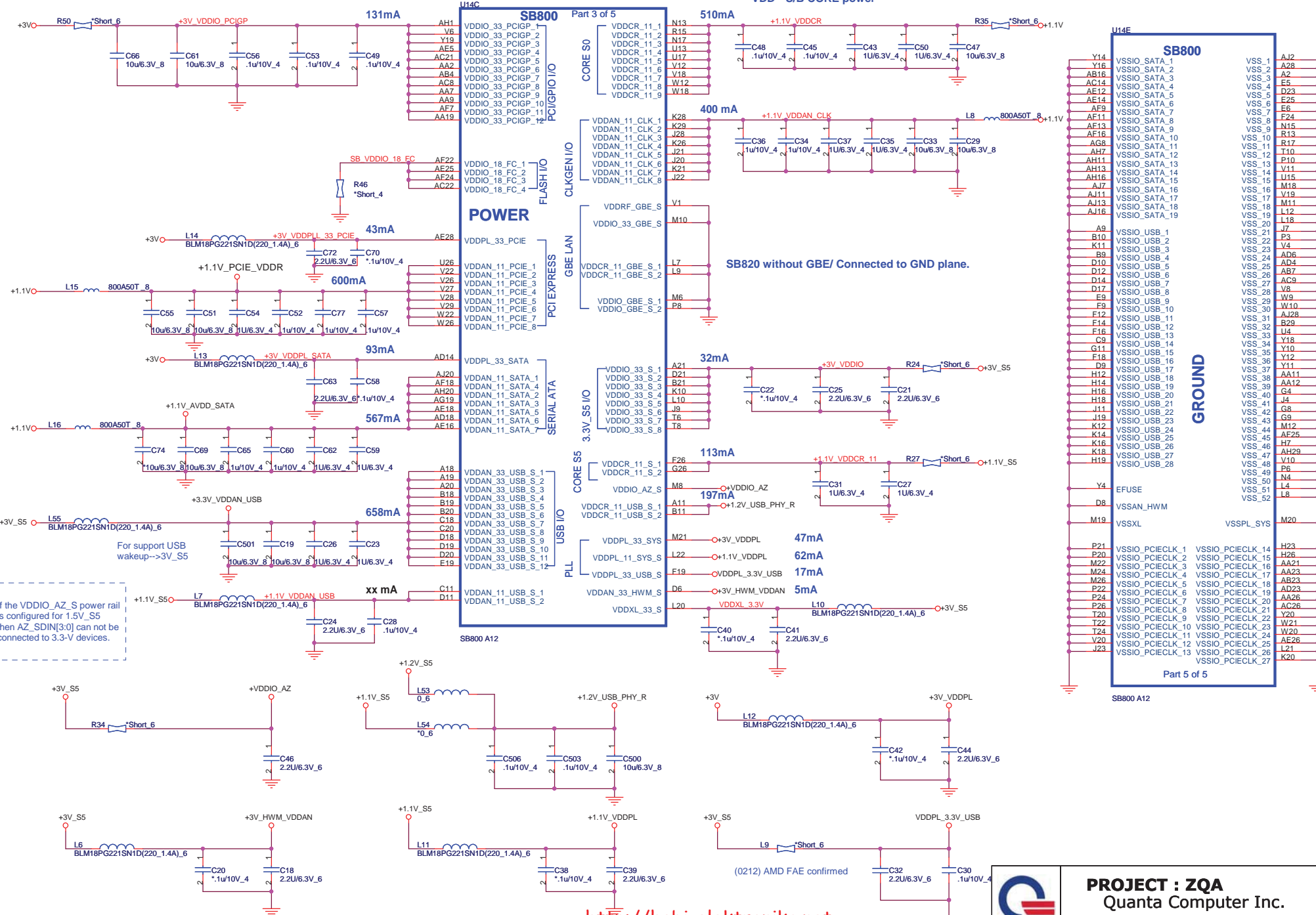
<http://hobi-elektronika.net>

www.vinafix.vn

VDDQ--3.3V I/O power

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power



<http://hobi-elektronika.net>

www.vinafix.vn



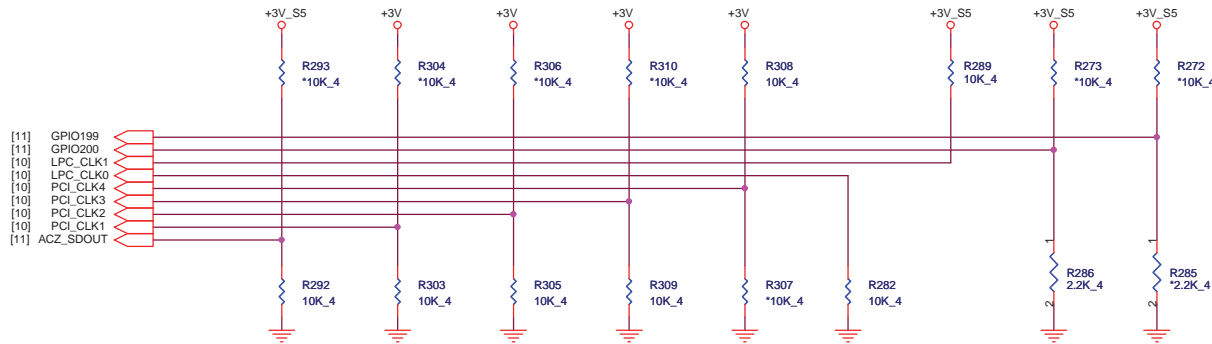
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number SB820-PWR/DECOUPLING 4/4	Rev 1A
Date:	Monday, May 31, 2010	Sheet 13 of 48

REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

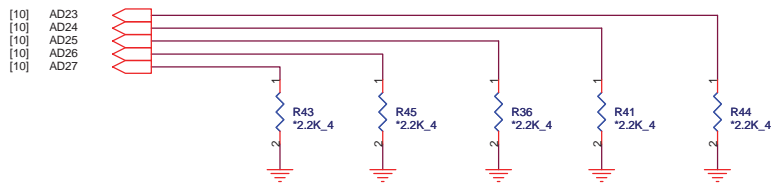


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM	

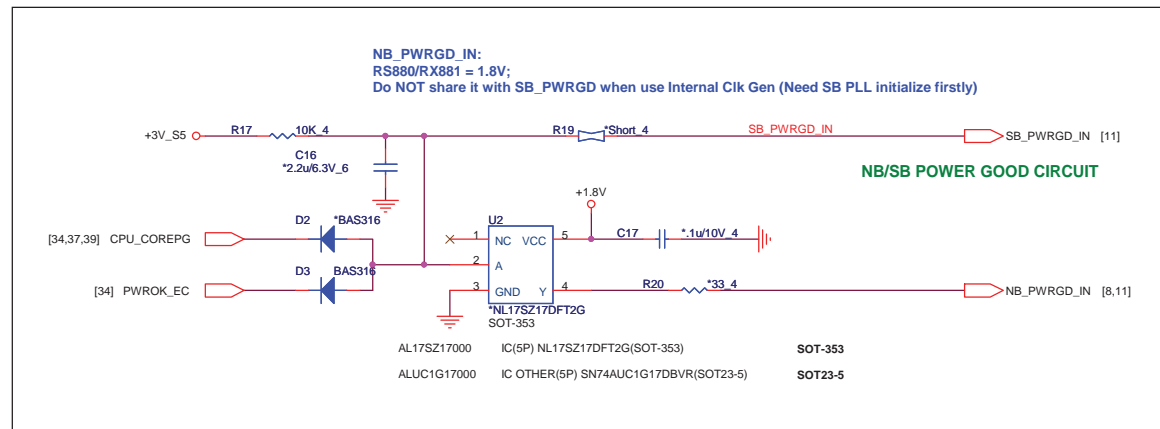
internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

14



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number SB820-STRAPS	Rev 1A
Date: Monday, May 31, 2010	Sheet 14	of 48

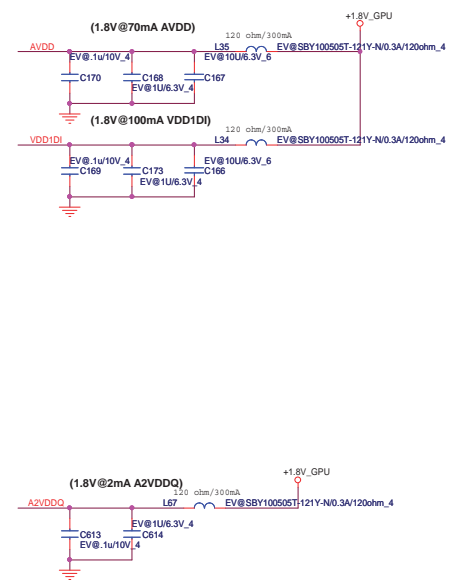
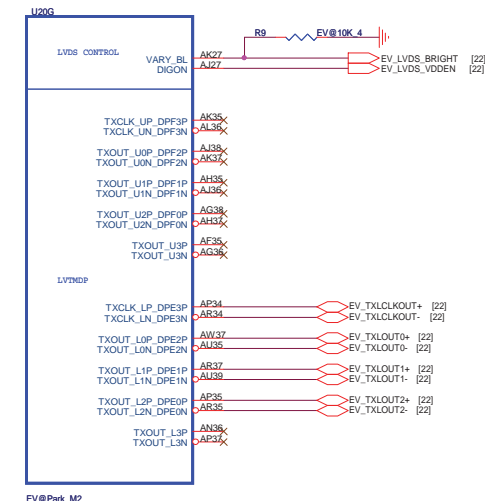
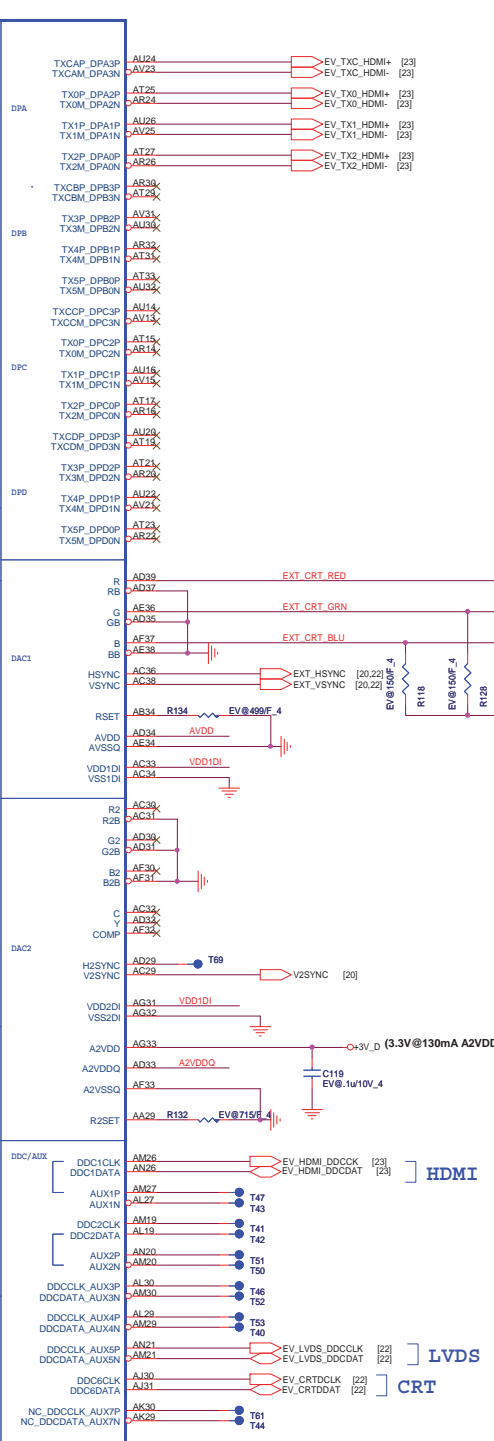
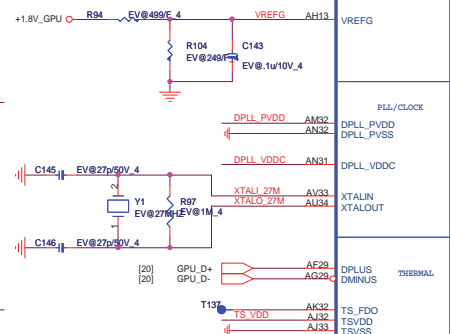
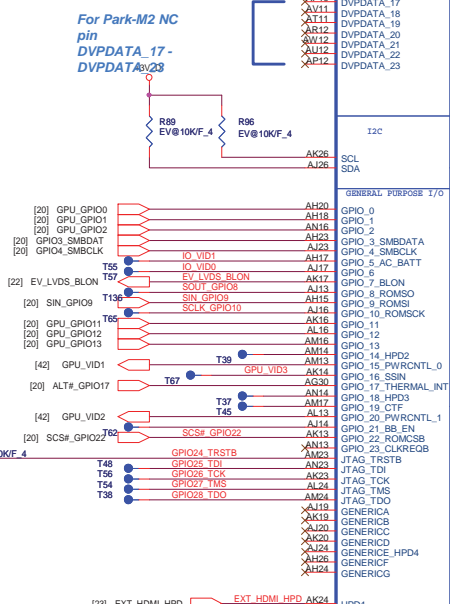
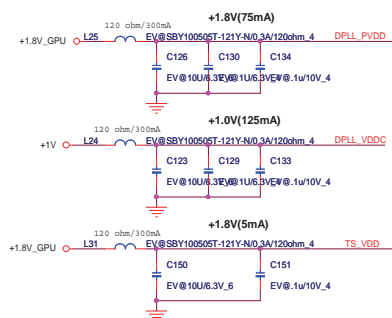






GPU Power-on sequence


- 1 => +3V_D
- 2 => +VGPU_CORE
- 3 => +1V
- 4 => +1.5V_GPU
- 5 => +1.8V_GPU
- 6 => dGPU_PWROK

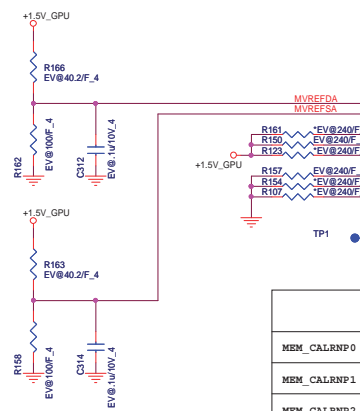
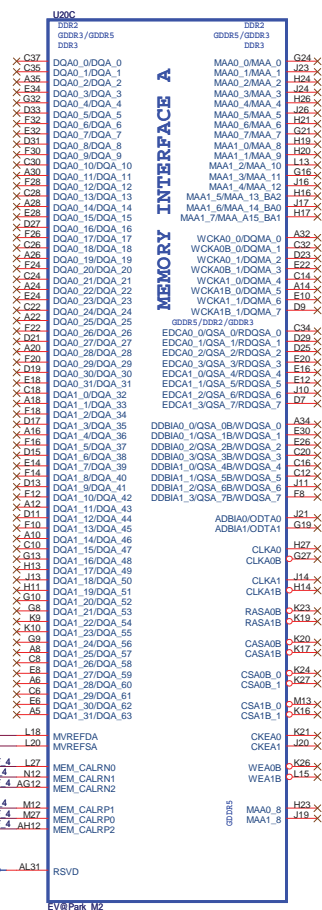
1.8V GPIO

3.3V GPIO



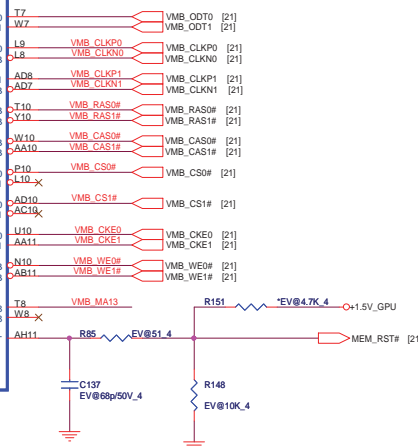
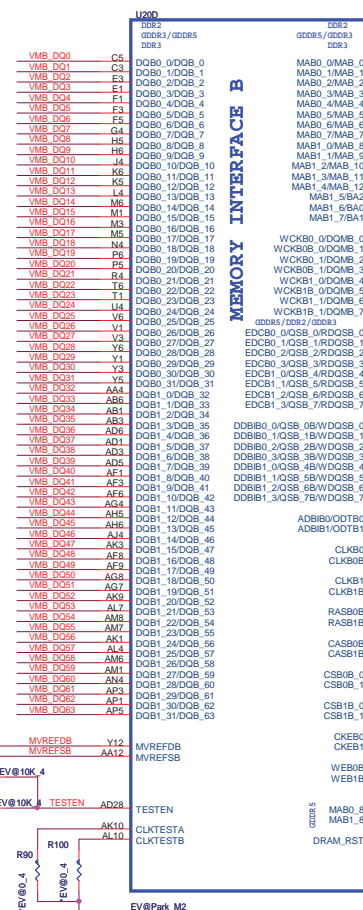
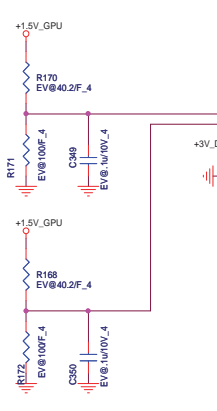
[21] VMB_DQ[63..0]  VMB_DQ[63..0]
[21] VMB_DM[7..0]  VMB_DM[7..0]
[21] VMB_RDQS[7..0]  VMB_RDQS[7..0]
[21] VMB_WDQS[7..0]  VMB_WDQS[7..0]

[21] VMB_MA[13..0]  VMB_MA[13..0]



DDR3/GDDR3 Memory Stuff Option

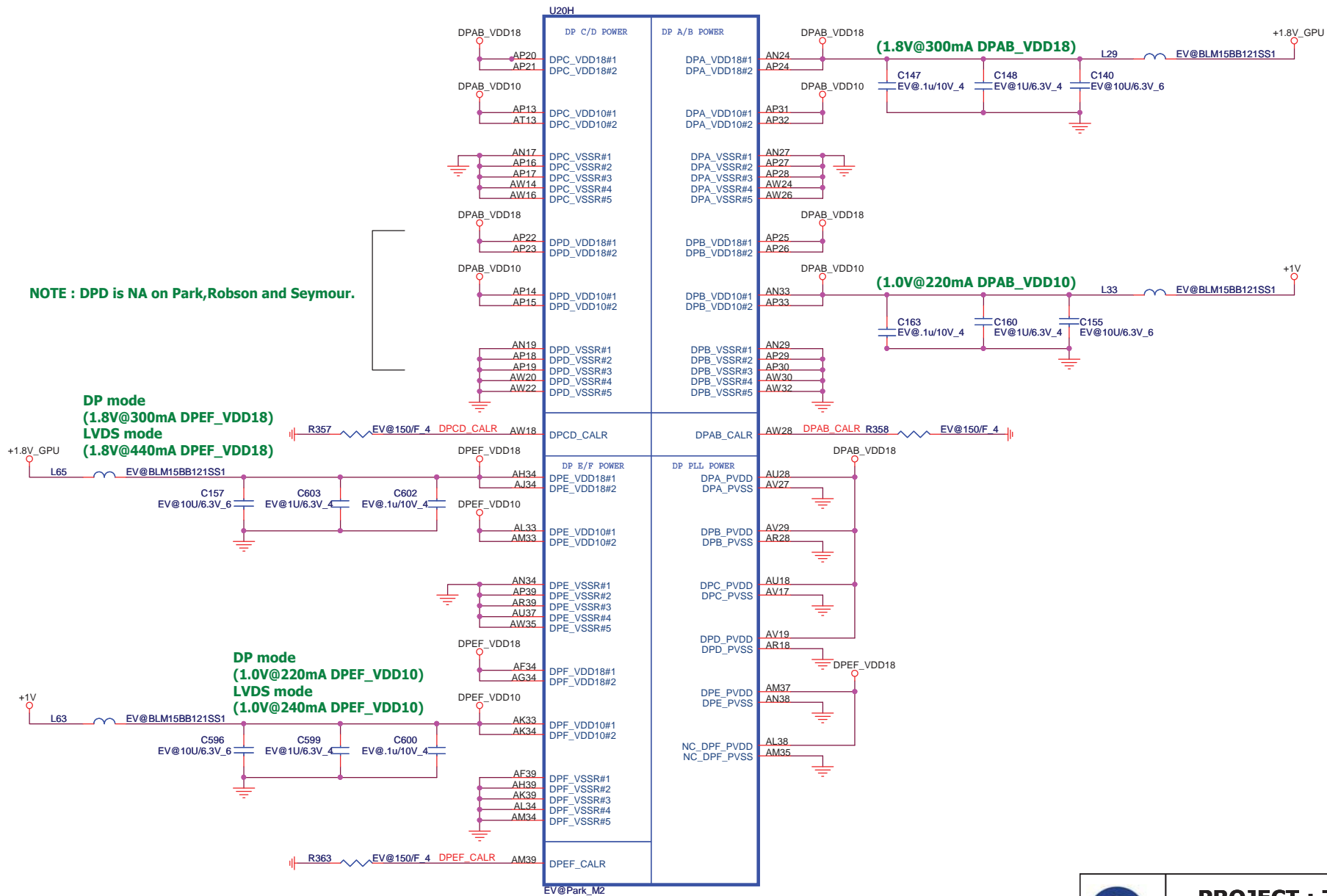
	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Designator	For M97-M2	For Mannhatto
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF



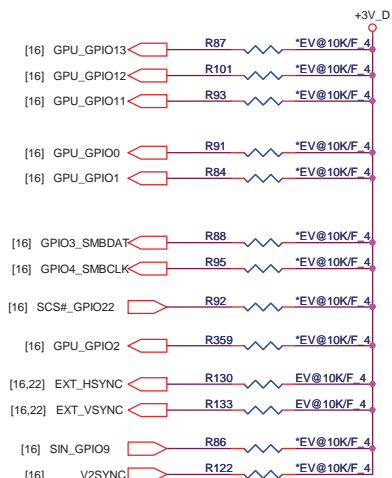




PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number Madison/Park (DP_PWR/GND)5/6	Rev 1A
Date:	Monday, May 31, 2010	Sheet 19 of 48

PIN STRAPS



Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table

EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

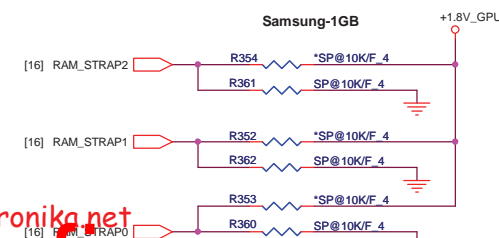
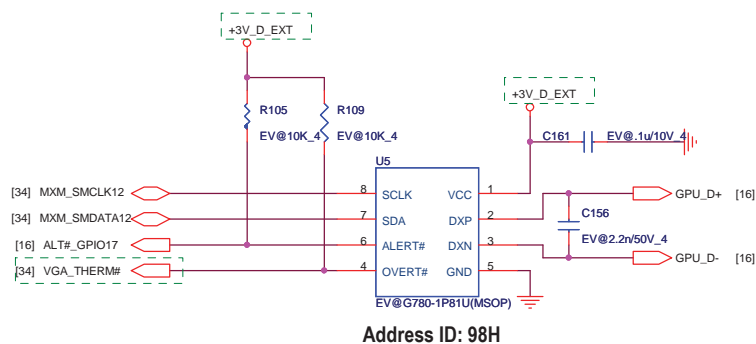
20

DDR3 Memory Aperture size


DDR3 Memory Aperture size

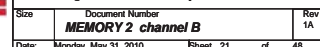
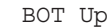
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVDPDATA_2	RAM_STRAP1 DVDPDATA_1	RAM_STRAP0 DVDPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	1	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1

Thermal Sensor



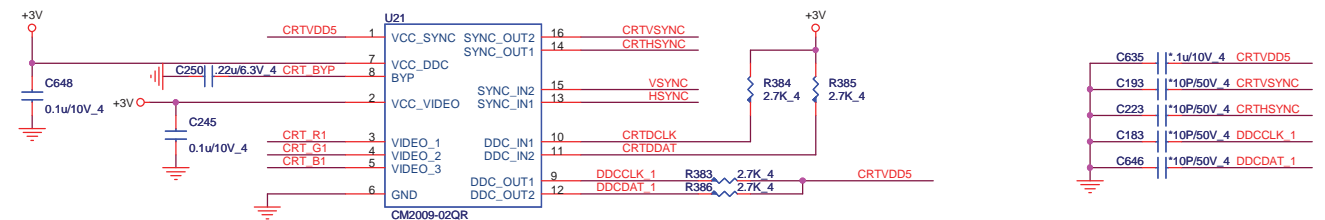
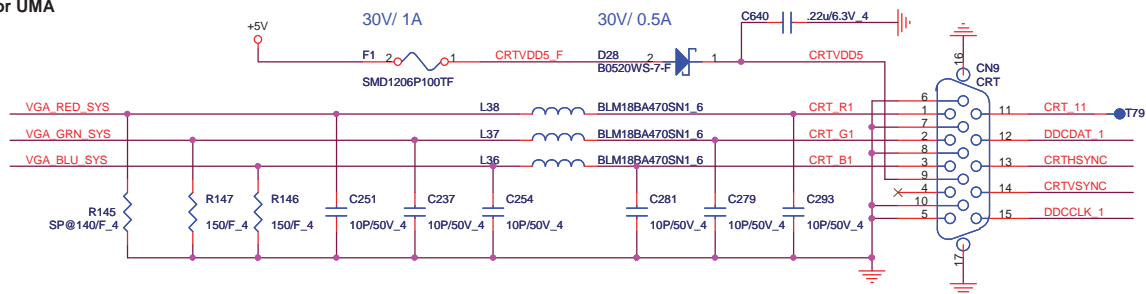
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

 PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number	Rev 1A
Date: Monday, May 31, 2010	Medison/Park Strip/Thermal 6/6	
Sheet 20	of 48	

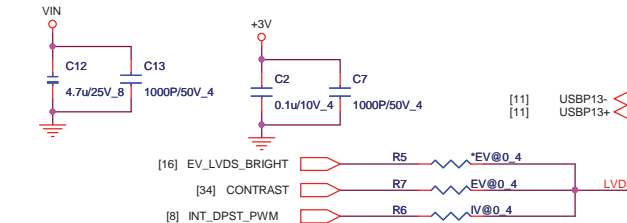
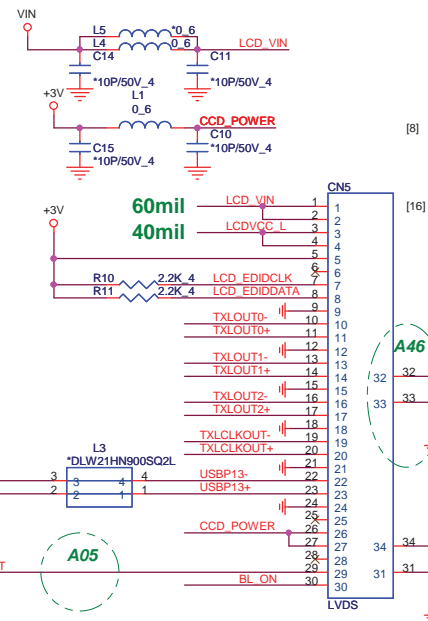
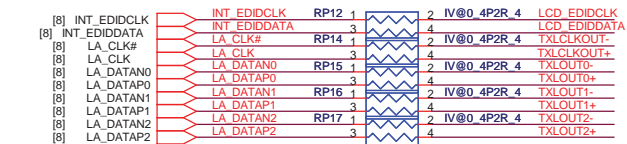


OPTION SIGNAL FROM NB to LVDS/CRT for UMA

[8]	INT_DDCCLK	INT DDCCLK	RP2	3	4	IV@0.4P2R	4	CRTDCLK
[8]	INT_DDCDATA	INT DDCDATA						CRTDCLK
[8]	INT_CRT_HSYNC	INT CRT HSYNC	RP5	3	4	IV@0.4P2R	4	HSYNC
[8]	INT_CRT_VSYNC	INT CRT VSYNC						VSYNC
[8]	INT_CRT_RED	INT CRT RED	R125			IV@0.4		VGA RED SYS
[8]	INT_CRT_GRE	INT CRT GRE	R121			IV@0.4		VGA GRN SYS
[8]	INT_CRT_BLU	INT CRT BLU	R117			IV@0.4		VGA BLU SYS



LVDS(LDS) OPTION SIGNAL FROM NB to LVDS for UMA



Schematic diagram of the HE1 AH9249NTR-G1 SOT23-123-2, 8-1_9. The diagram shows a power supply section with a +3VPCU input, a 1u6.3V capacitor (C495), and a resistor R251 labeled *470K/F_4. The output is labeled LID591#.

PT3661-BB (PLC) : AL003661003
ME268-002 (FCE) : AL000268000

[illegible]

The schematic diagram illustrates the LED driver circuit. It is powered by a +3V supply. The circuit includes three MOSFETs: Q1 (2N7002K), Q2 (DTC144EUA), and Q3 (2N7002K). Q1 and Q2 are configured as a current source and a current mirror, respectively, to regulate the LED current. Q3 is the main switching MOSFET. The LED (LID591#) is connected in series with a diode (D1, BAS316) and a resistor (R12, 10K_4) to the +3V supply. The feedback signal (EC_FPBACK#) is taken from the LED current sense resistor (R13, 10K_4). The input signals are INT_LVDS_BLO# and EV_LVDS_BLO#, which are connected to the gates of Q1 and Q3 through resistors R16 and R14, respectively. A resistor R15 (100K_4) is connected between the gates of Q1 and Q3. The LED current is set by the ratio of R13 to R12, and the feedback signal is proportional to the LED current.



PROJECT : ZQA
Quanta Computer Inc.

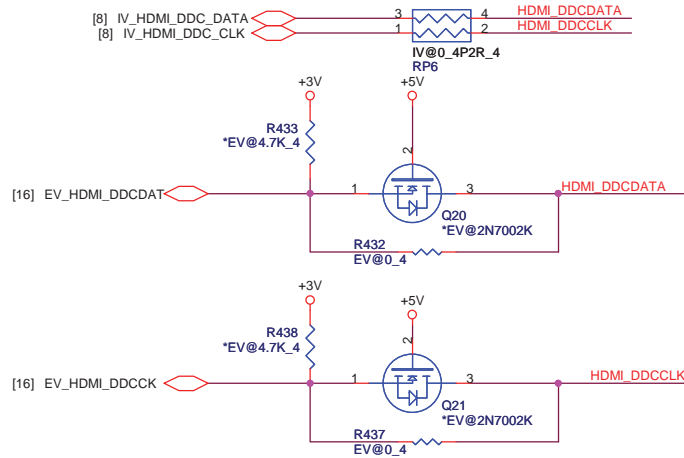
Size	Document Number CRT/LVDS/LID	Rev 1A
Date:	Monday, May 31, 2010	Sheet 22 of 48

HDMI SDVO I2C Control

UMA

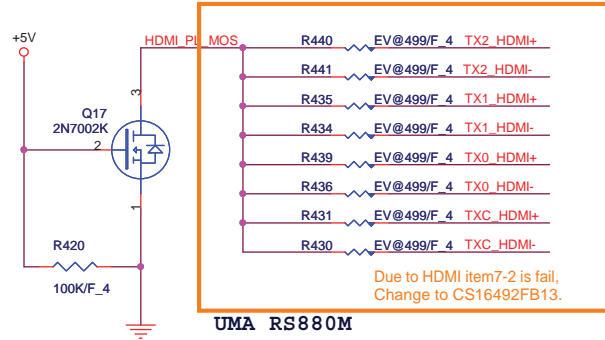
Close to HDMI Connector

DIS



HDMI (HDM)

Close to HDMI Connector



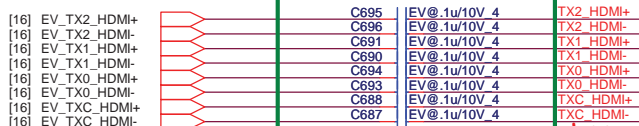
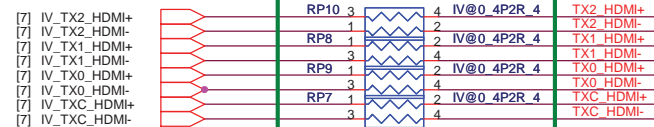
UMA RS880M

Stuff 715 ohm CS17152FB17

DIS Park-M2

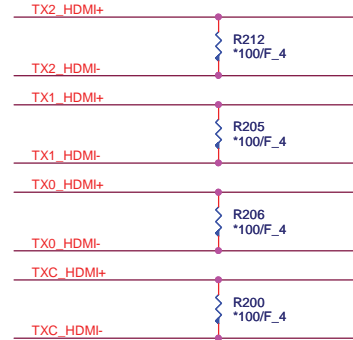
Stuff 499 ohm CS14992FB24

for Layout concern
,placement close HDMI conn

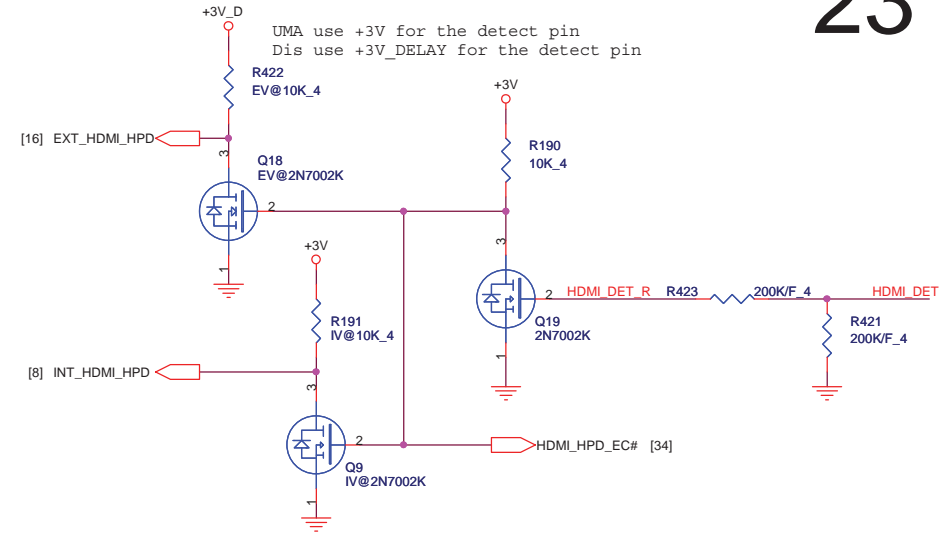


EMI reserve for HDMI(EMC)

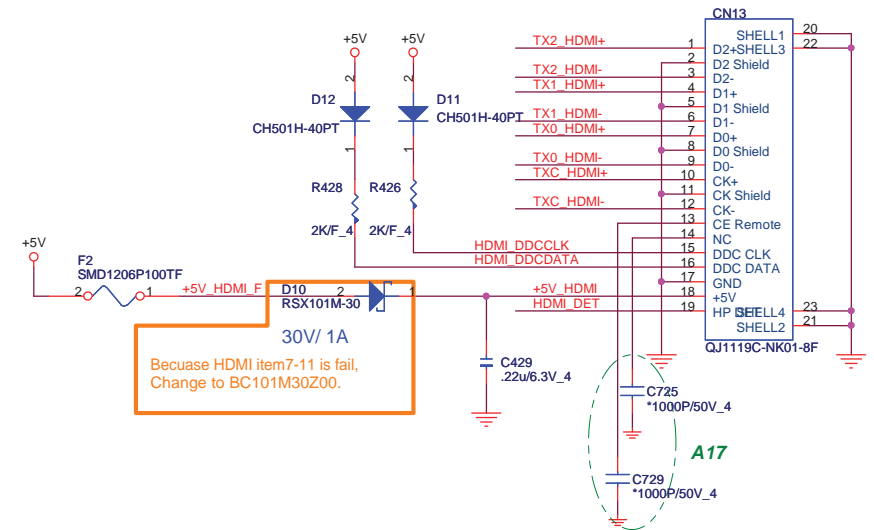
Close connector




HDMI HPD SENSE (HDM)



HDMI PORT (HDM)

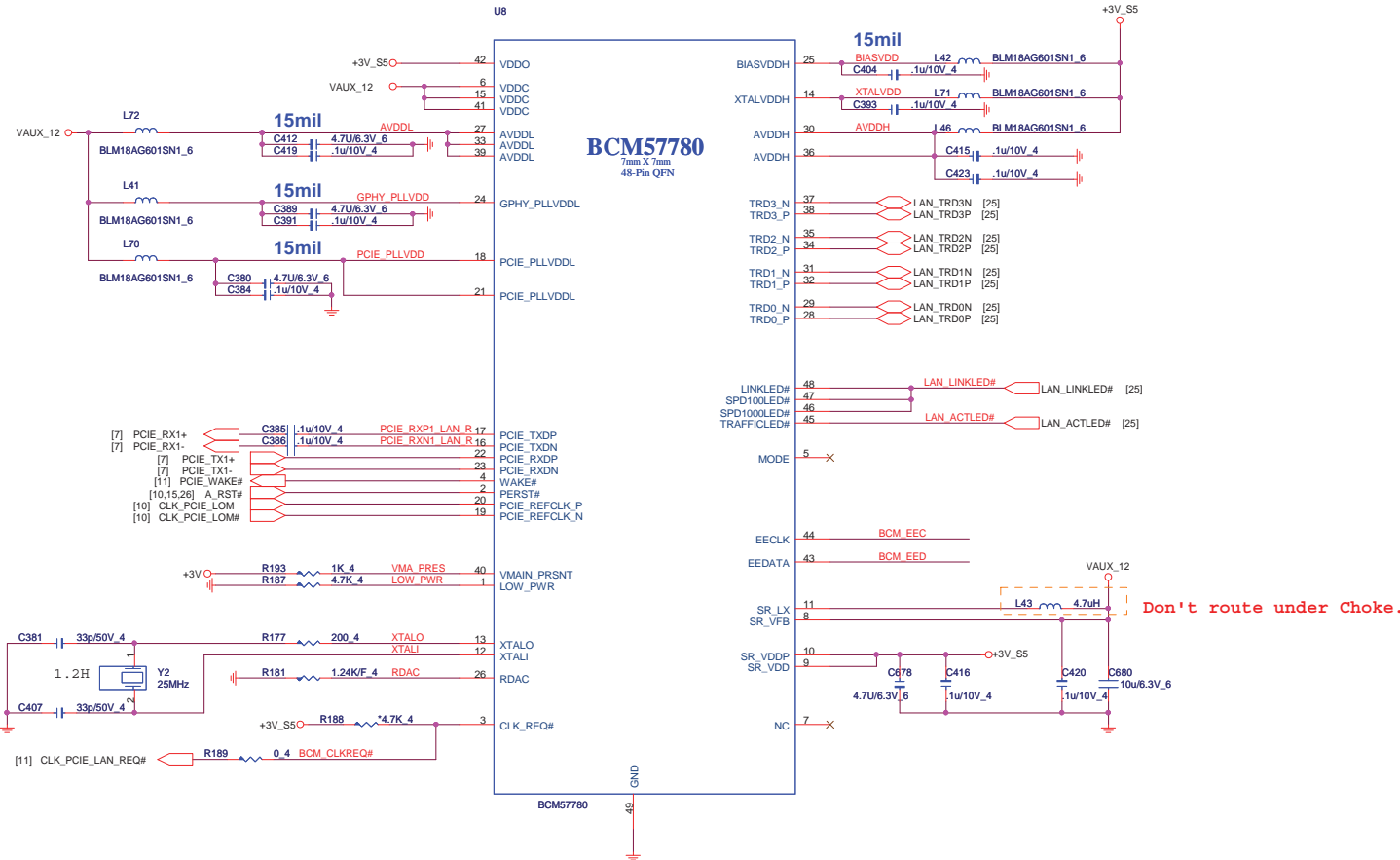


 PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number	Rev
	HDMI	1A
Date:	Monday, May 31, 2010	Sheet 23 of 48

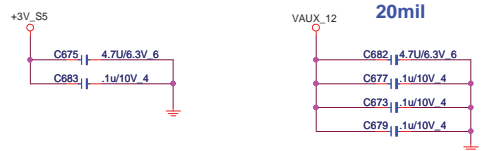
<http://hobi-elektronika.net>

www.vinafix.vn

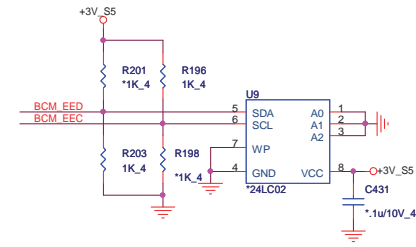
23



LAN POWER



EEPROM

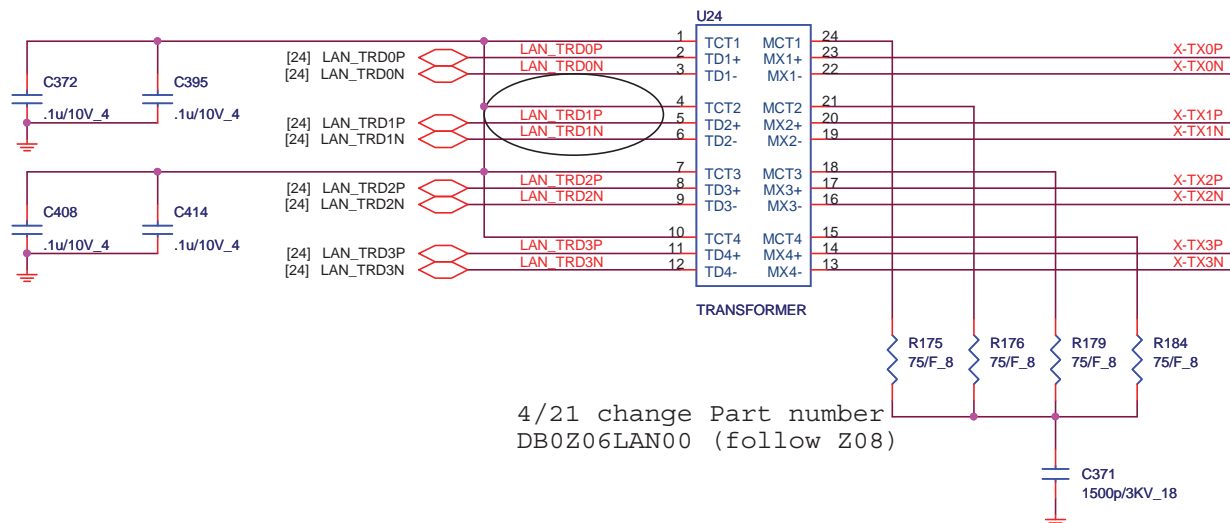


EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	0	0

TRANSFORMER

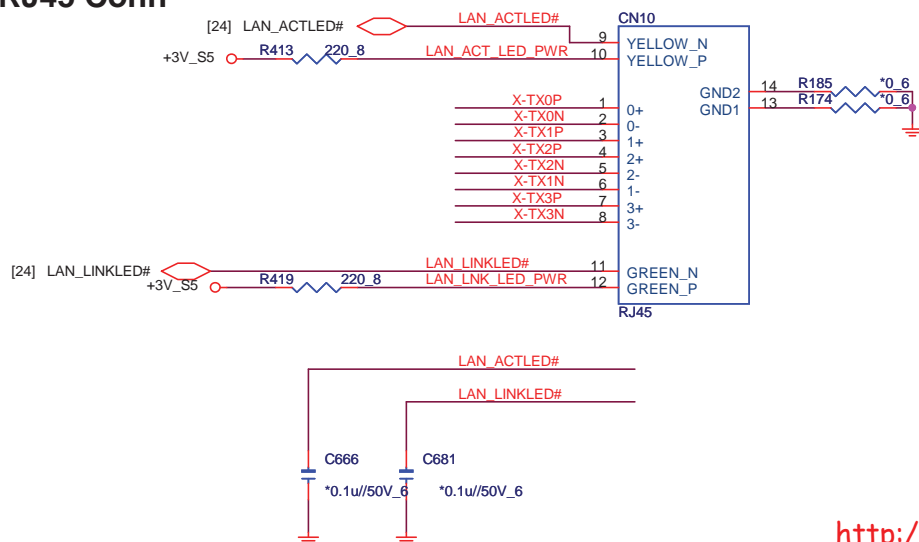
4/27 modify it



4/21 change Part number
DB0Z06LAN00 (follow Z08)

For EMI

RJ45 Conn



LAN_TRD0P	C378	*10P/50V_4
LAN_TRD0N	C388	*10P/50V_4
LAN_TRD1P	C399	*10P/50V_4
LAN_TRD1N	C402	*10P/50V_4
LAN_TRD2P	C410	*10P/50V_4
LAN_TRD2N	C413	*10P/50V_4
LAN_TRD3P	C417	*10P/50V_4
LAN_TRD3N	C421	*10P/50V_4



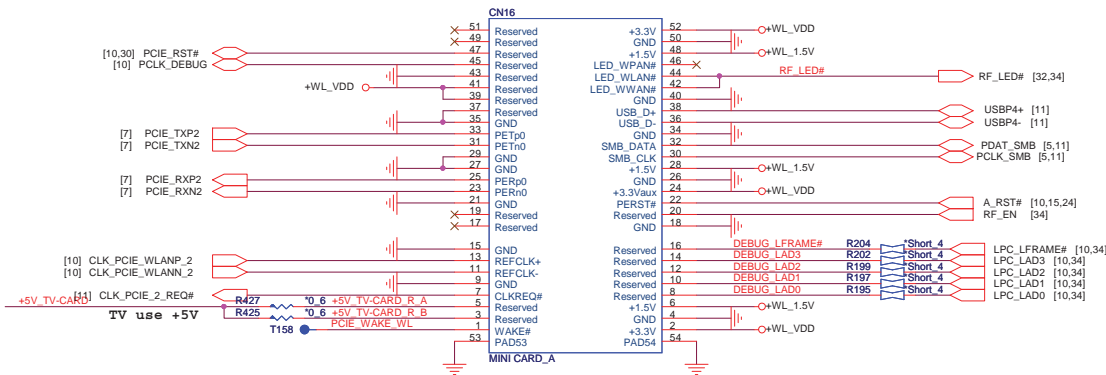
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	LAN Transformer and RJ45	1A
Date:	Monday, May 31, 2010	Sheet 25 of 48

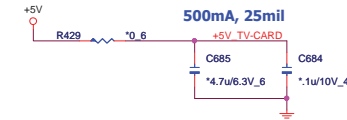
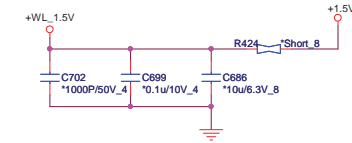
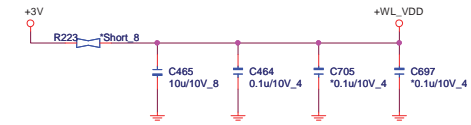
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)




Debug



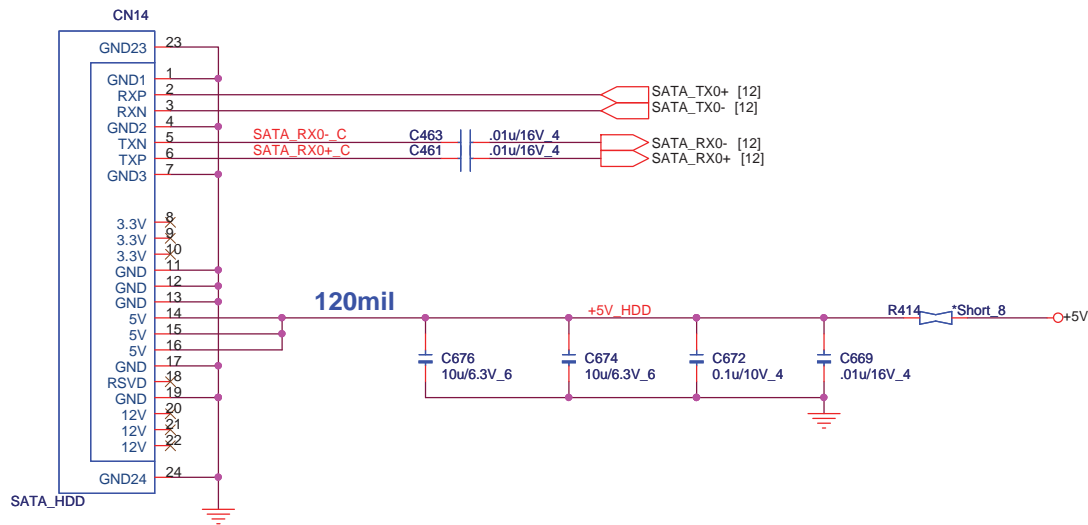
26

<http://hobi-elektronika.net>

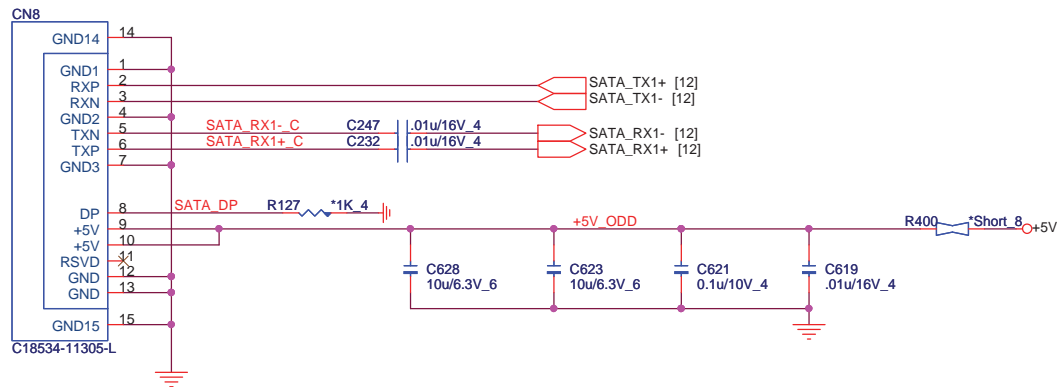
www.vinafix.vn


		PROJECT : ZQA	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	MINI PCI-E card/TV	1A	
Date:	Monday, May 31, 2010	Sheet	26 of 48

SATA HDD

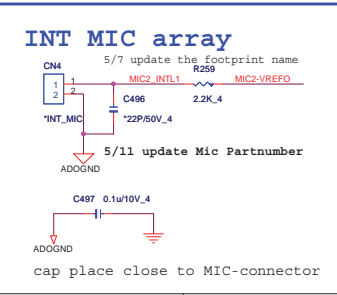
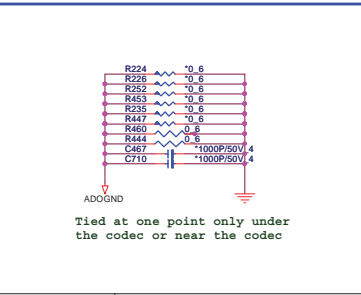
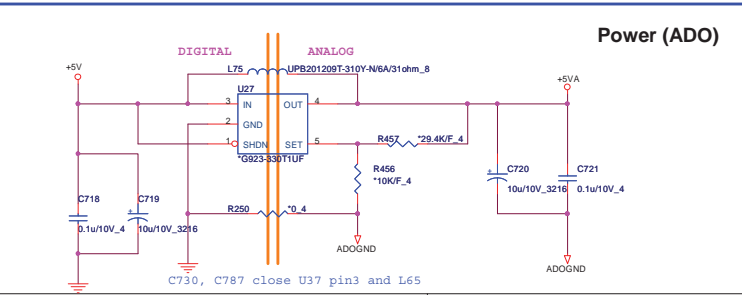
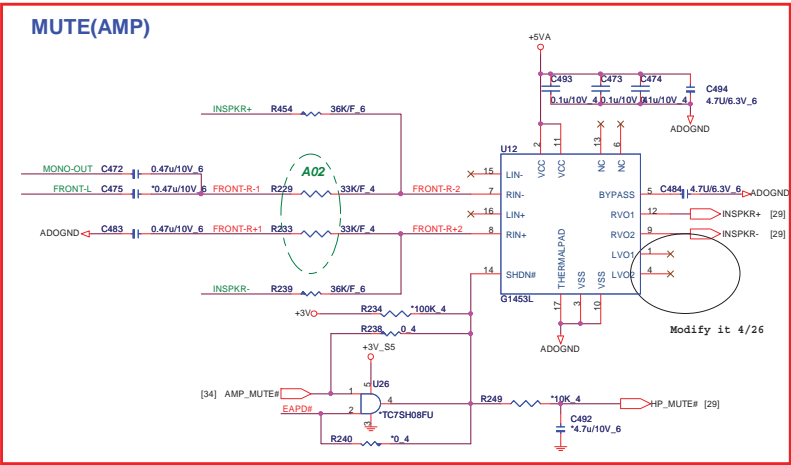
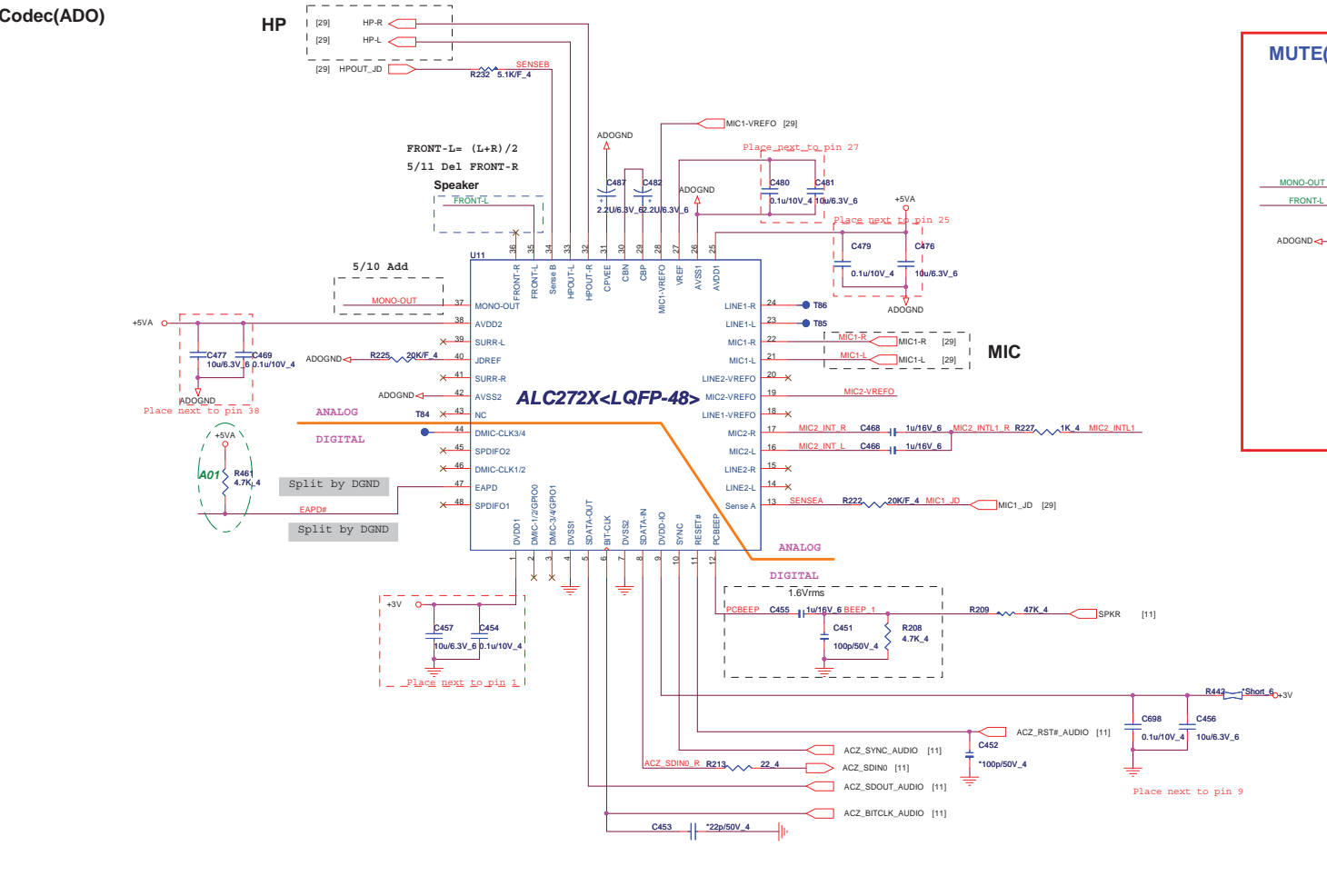


SATA ODD



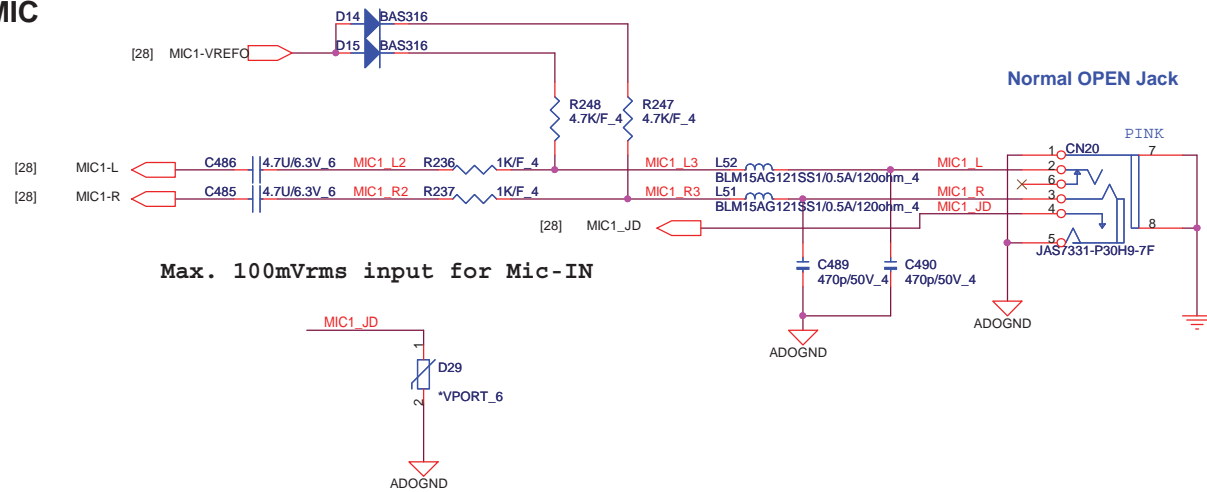
 PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number SATA-HDD/ODD/HOLE	Rev 1A
Date: Monday, May 31, 2010	Sheet 27 of 48	

Codec(ADO)

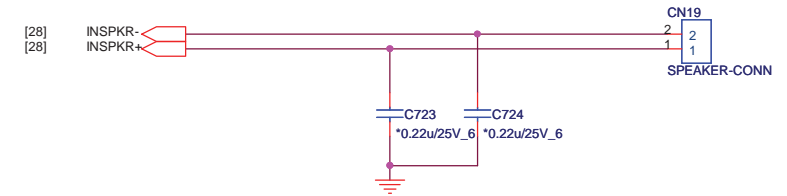


PROJECT : ZQA			
Quanta Computer Inc.			
Size	Document Number	Rev	
	REALTEK ALC663&888/MDC	1A	
Date:	Monday, May 31, 2010	Sheet	28 of 48

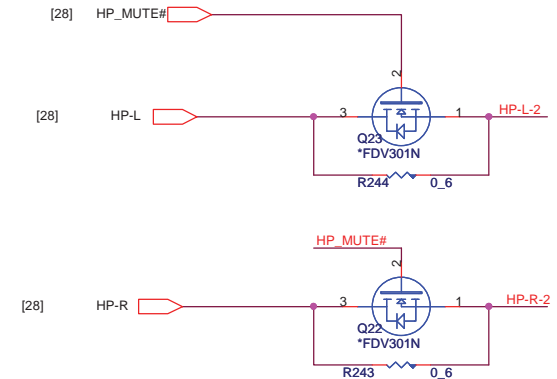
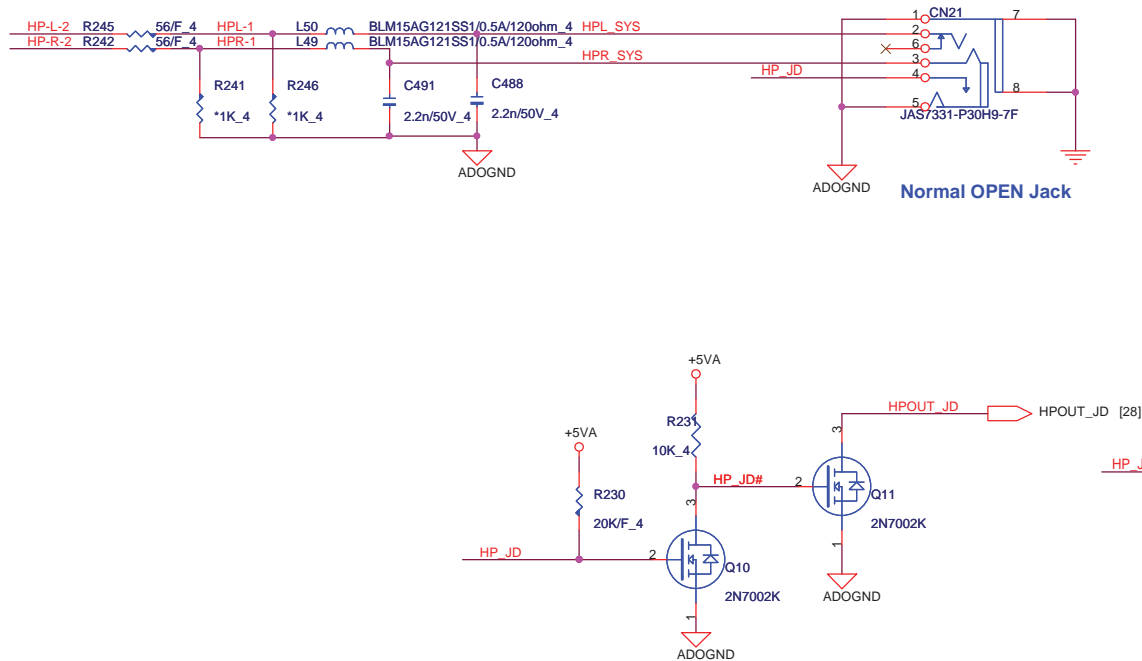
MIC



Internal Speaker



HP



PROJECT : ZQA
Quanta Computer Inc.

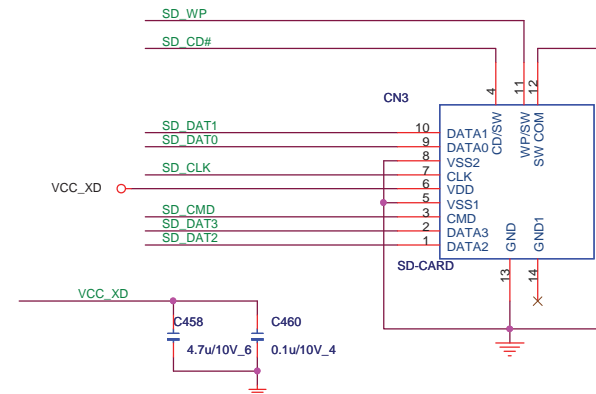
Size	Document Number AMP /AUDIO JACK CONN	Rev 1A
Date:	Monday, May 31, 2010	Sheet 29 of 48

CARD READER Controller

2 IN 1 CARD READER (MMC)

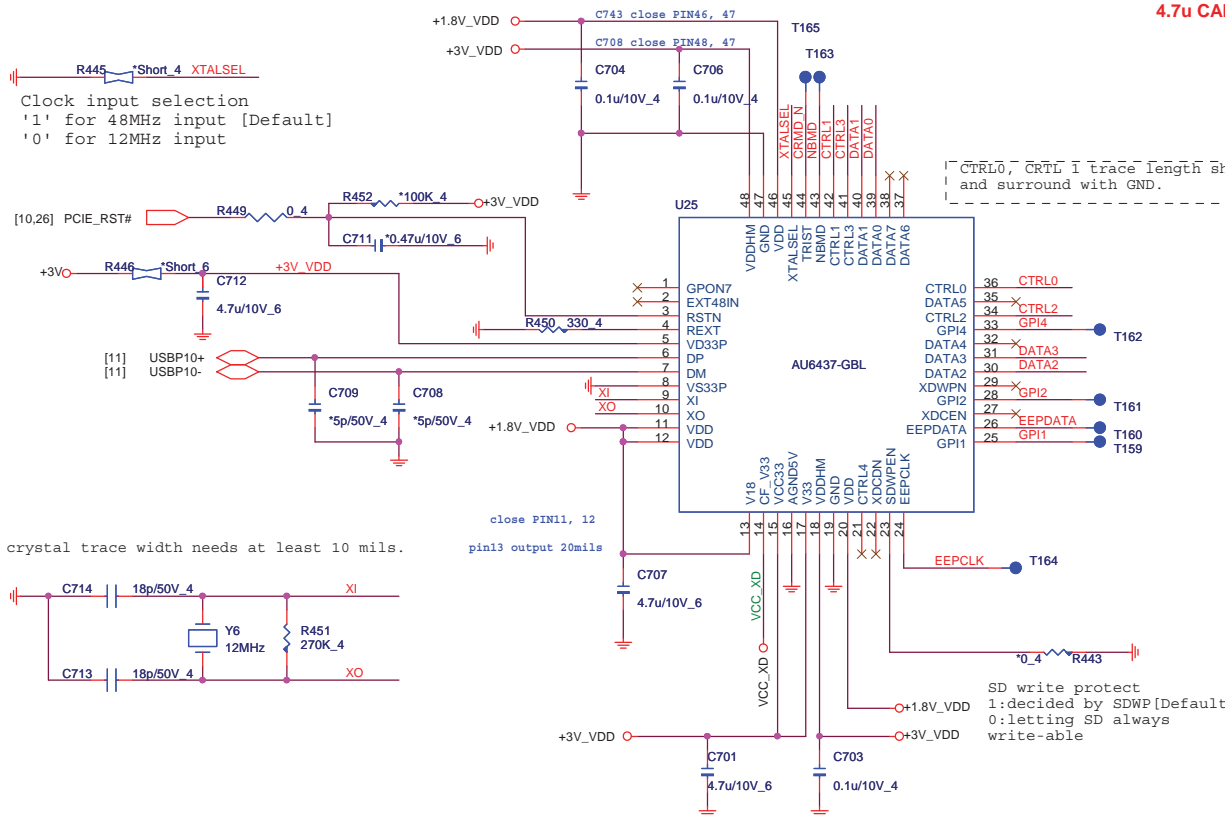
30

Main	DFHS11FR011
Second	DFHS11FR033

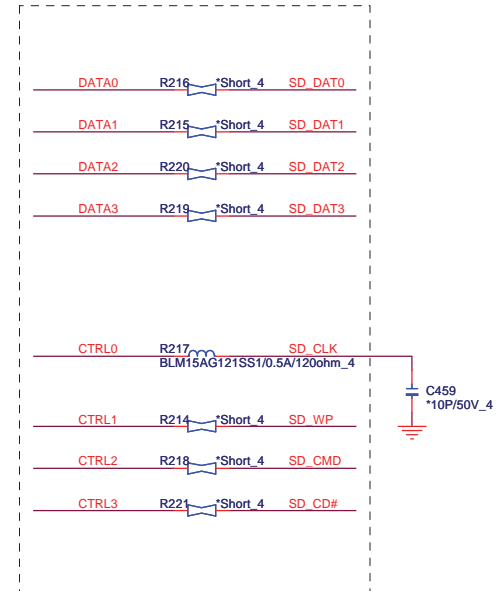


Close to CNxx pin 14 & pin23
4.7u CAP close to pin23

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt



CTRL0, CTRL1 trace length shorter,
and surround with GND.



crystal trace width needs at least 10 mils.

close PIN11, 12
pin13 output 20mils

SD write protect
1:decided by SDWP[Default]
0:letting SD always
write-able

<http://hobi-elektronika.net>

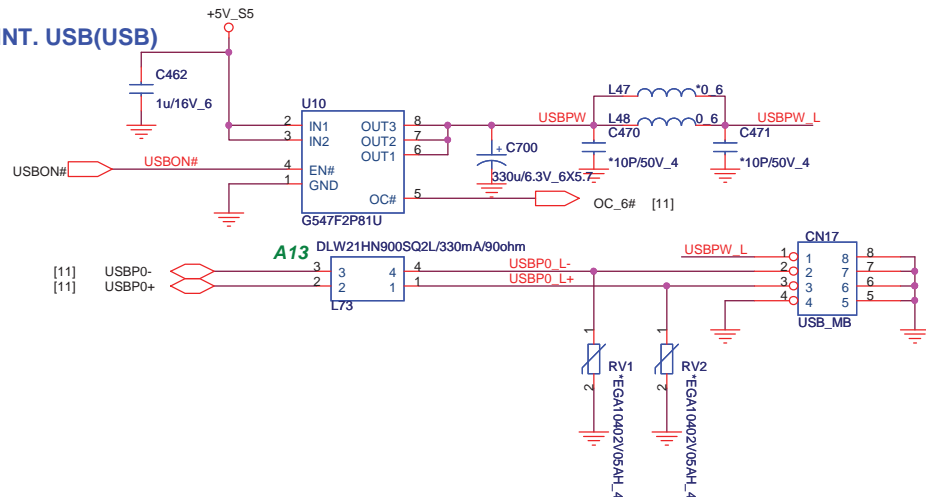
www.vinafix.vn



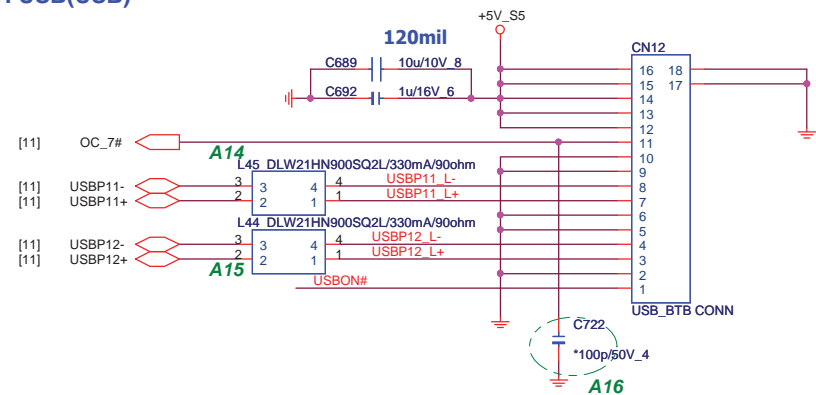
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date:	Monday, May 31, 2010	Sheet 30 of 48

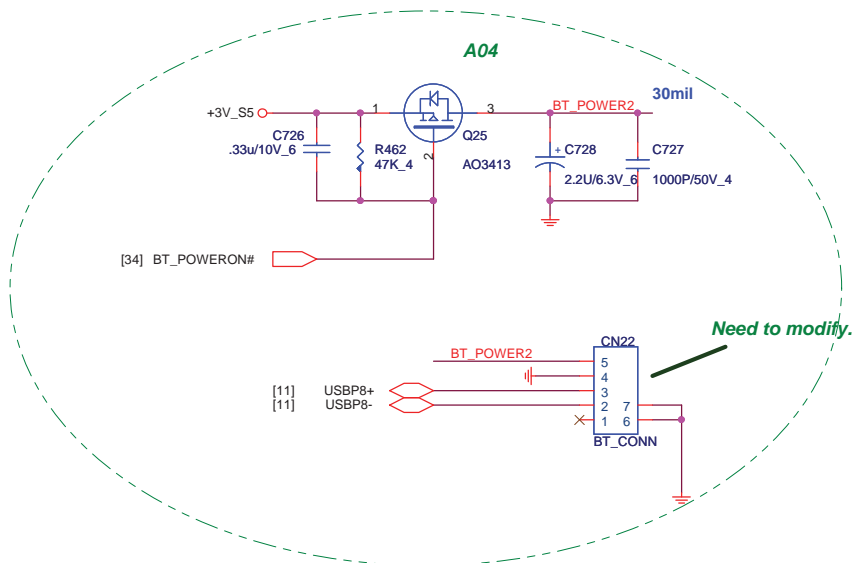
INT. USB(USB)



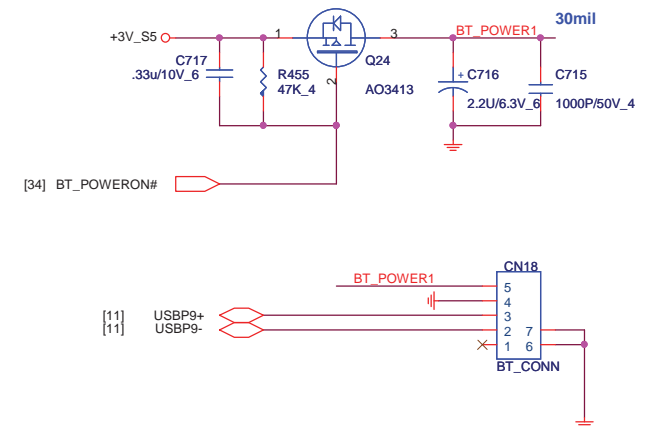
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



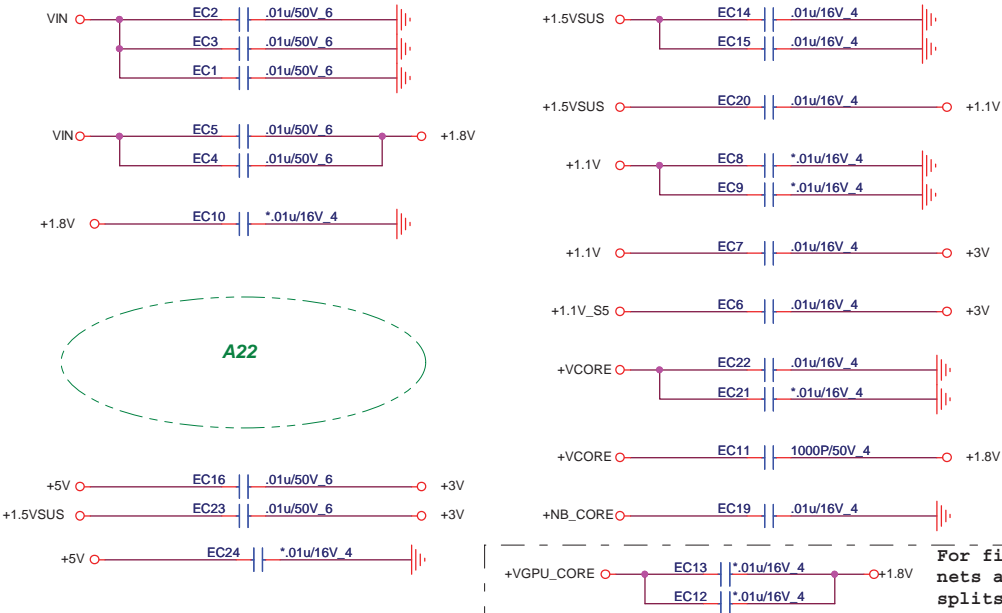
BLUETOOTH V3.0 CONN(BTM)



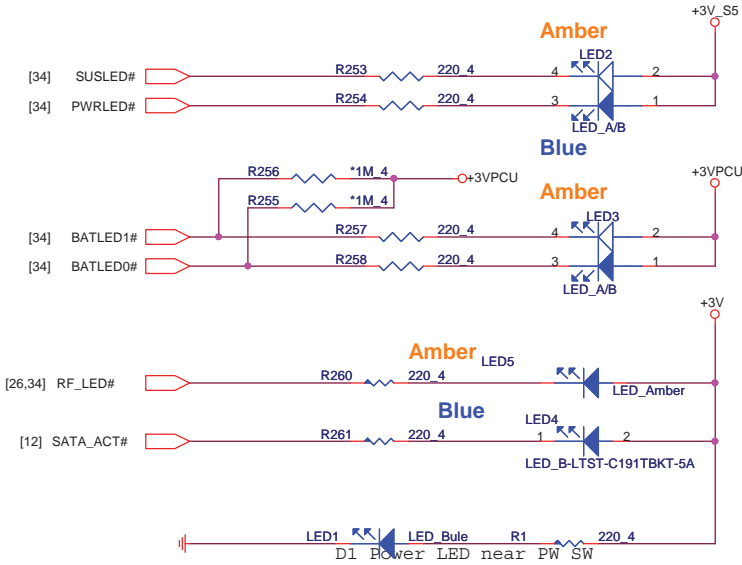
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT/TP	1A
Date:	Monday, May 31, 2010	Sheet 31 of 48

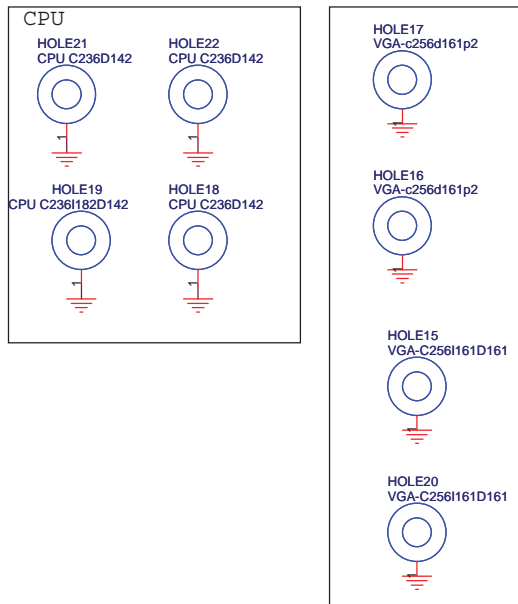
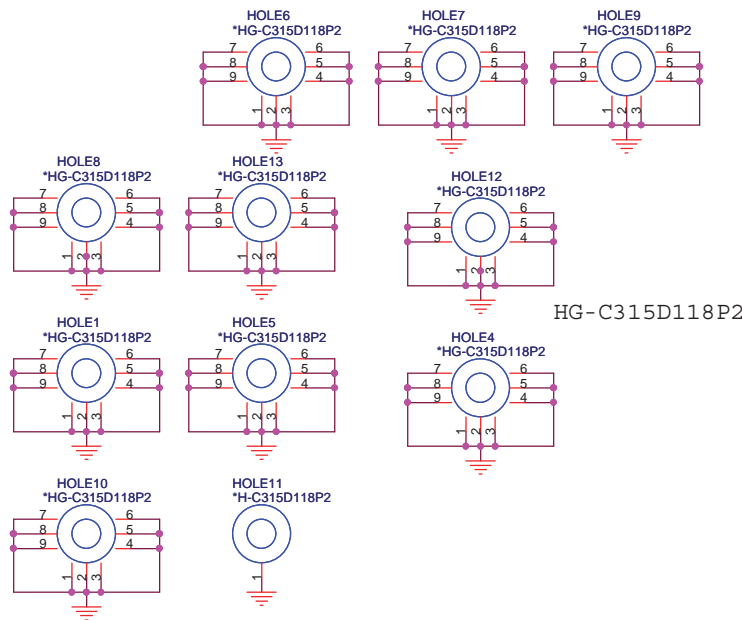
EE RETURN-PATH CAPACITORS(EMC)




LED(UIF)



HOLE(OTH)

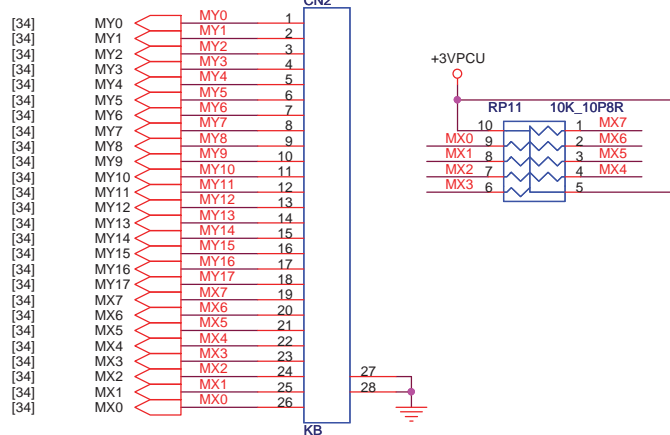




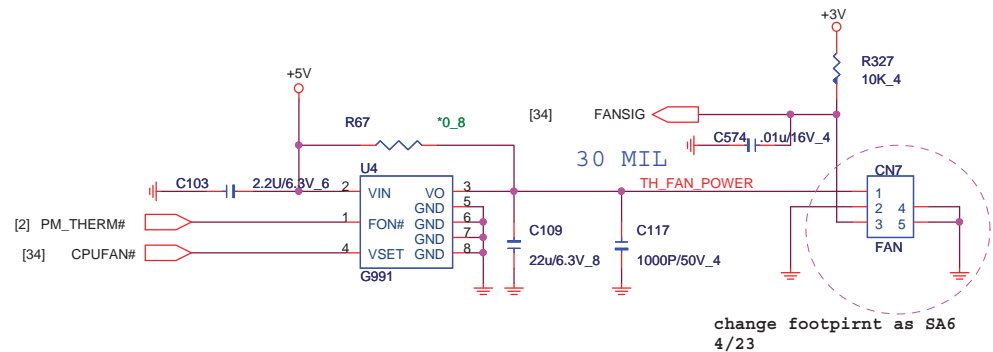
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
Date:	Monday, May 31, 2010	Sheet 32 of 48

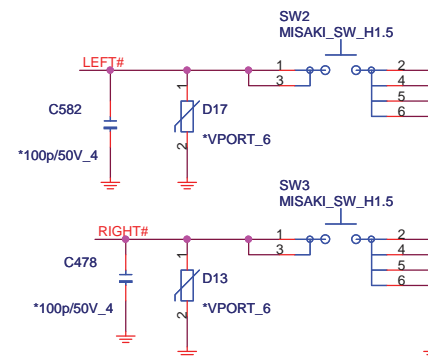
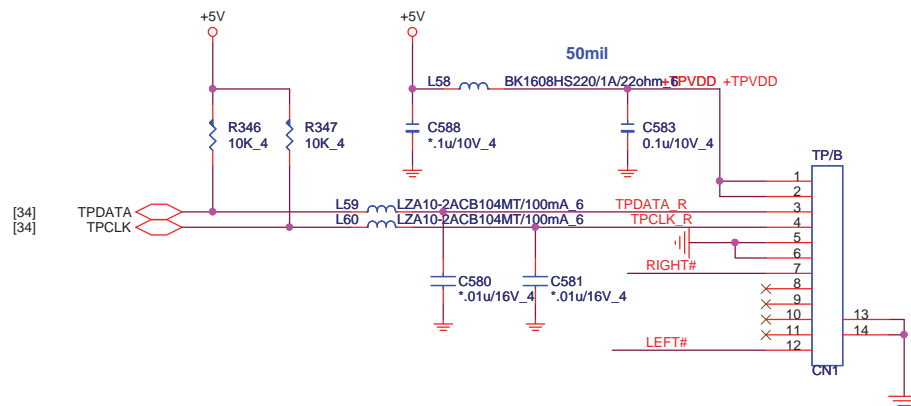
K/B(KBC)



CPU FAN(THM)

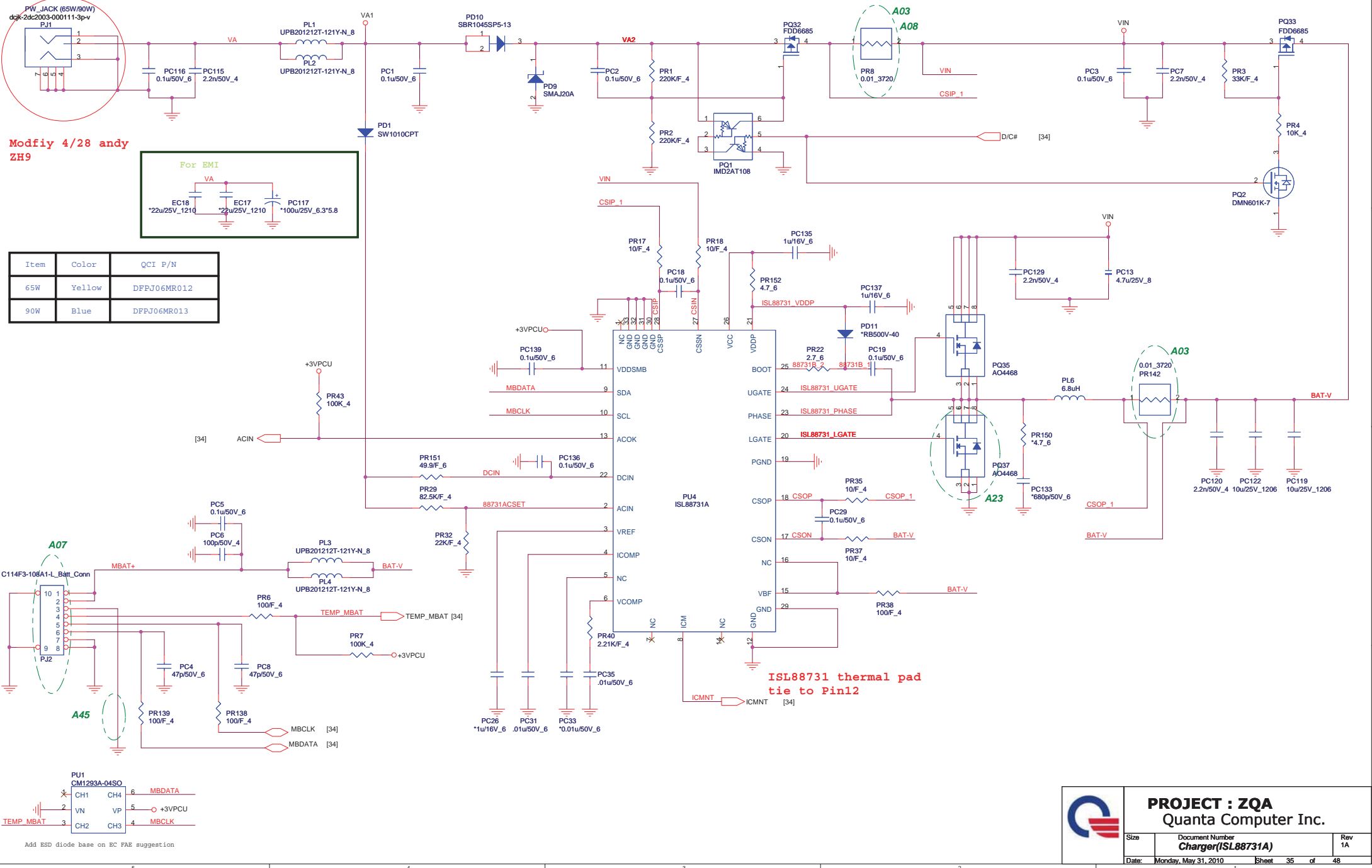


TOUCHPAD BOARD CONN(TPD)



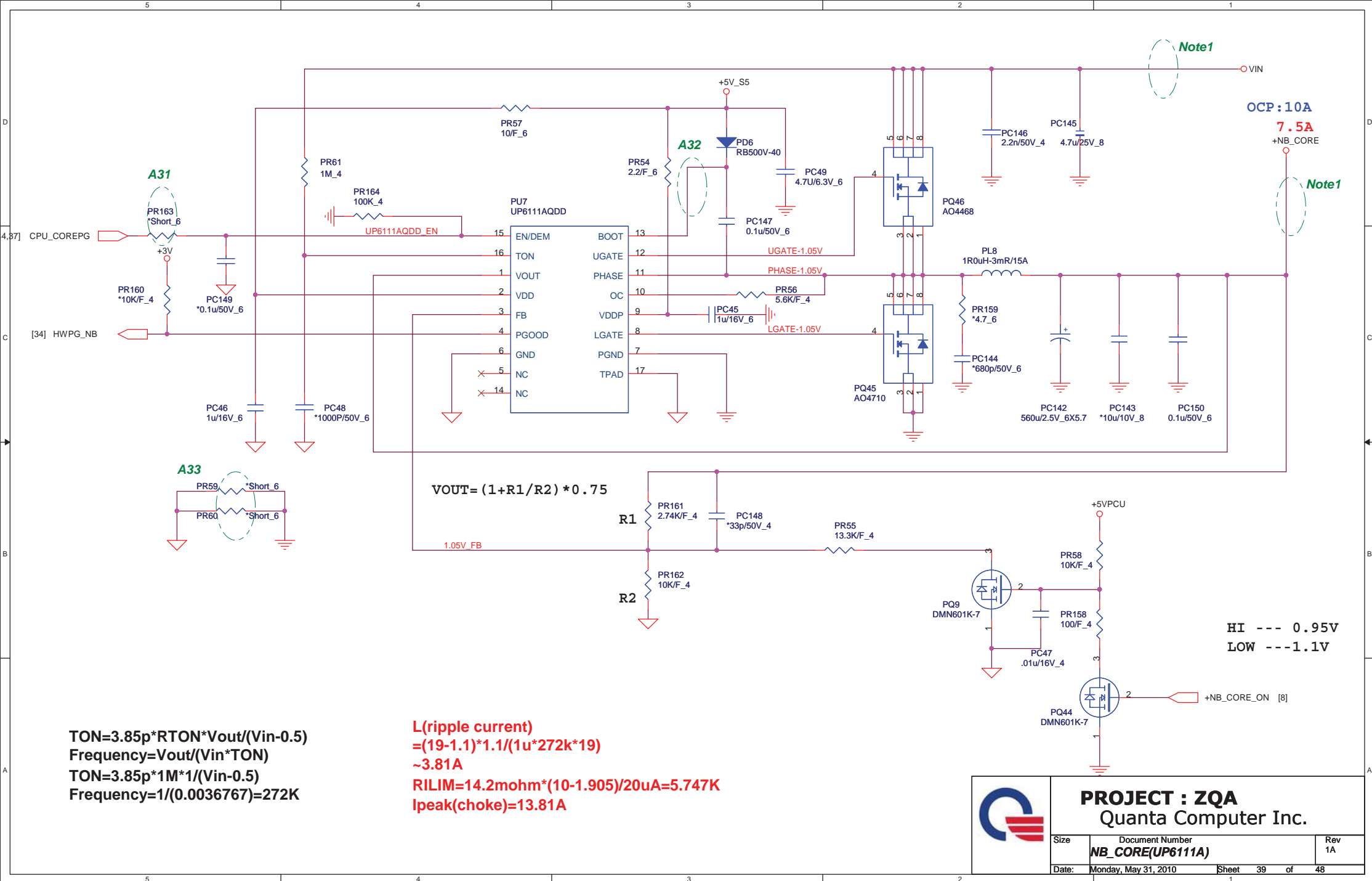
PROJECT : ZQA
Quanta Computer Inc.

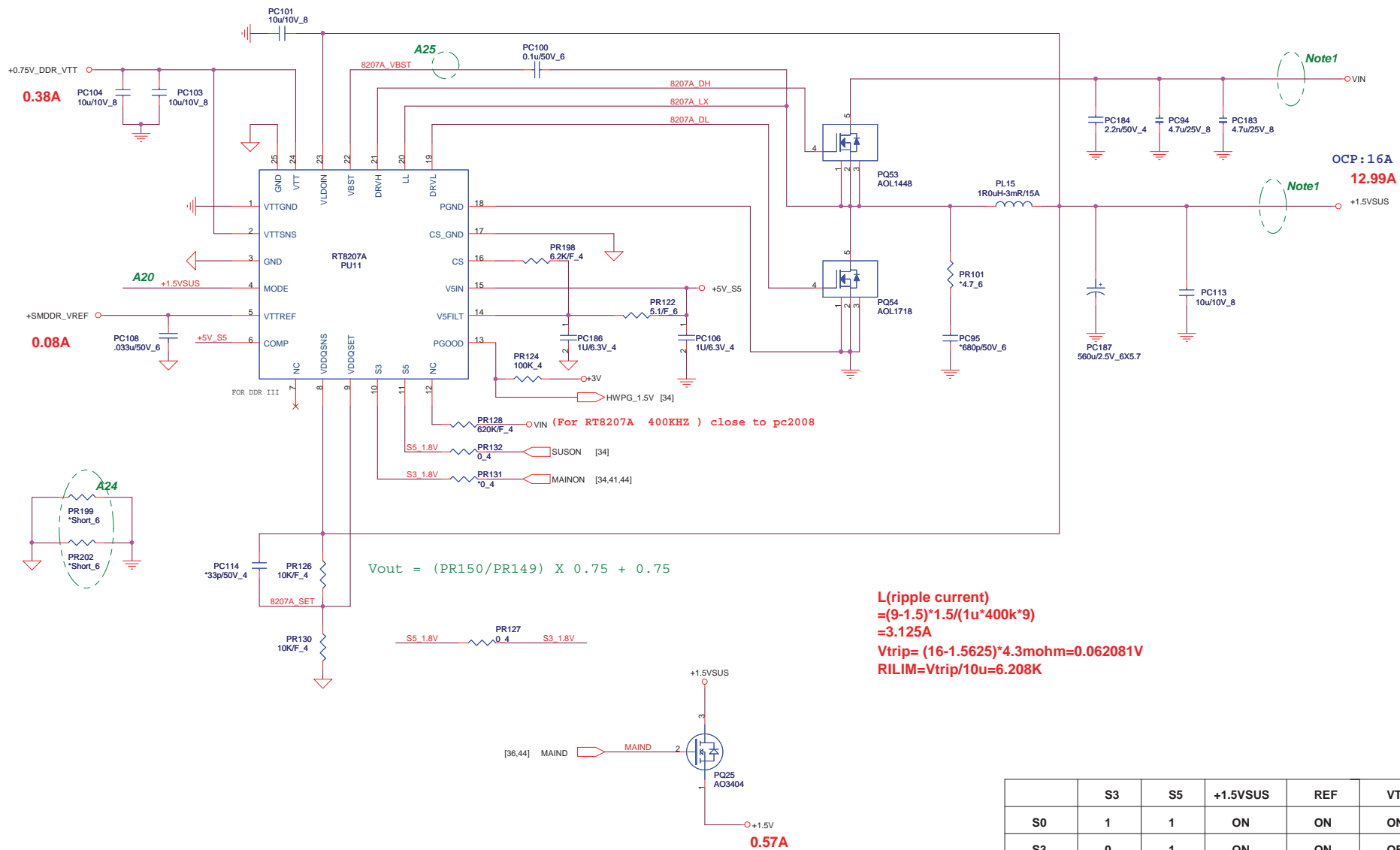
Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
Date:	Monday, May 31, 2010	Sheet 33 of 48



SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





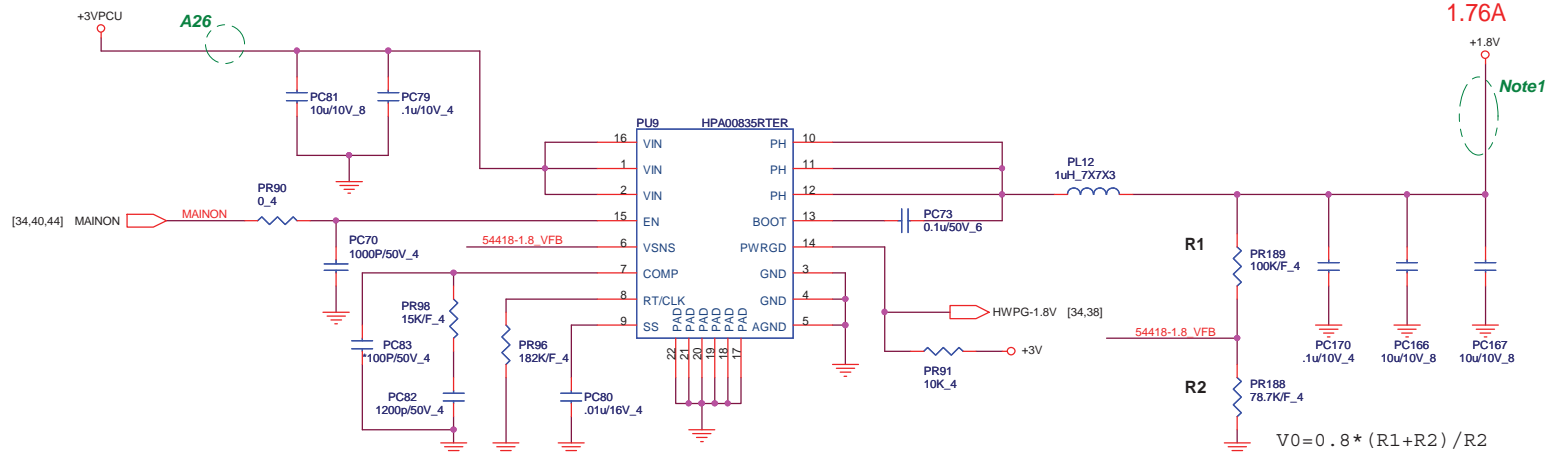
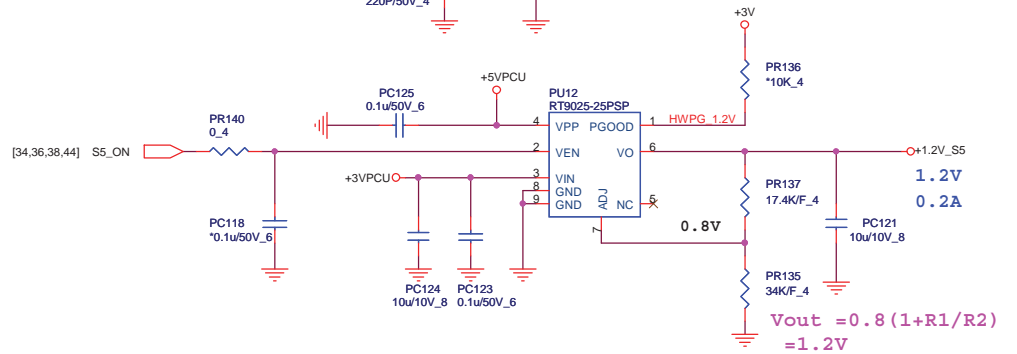
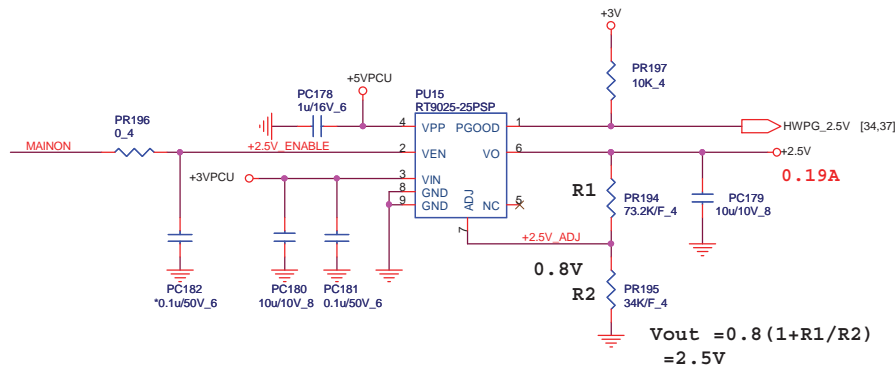
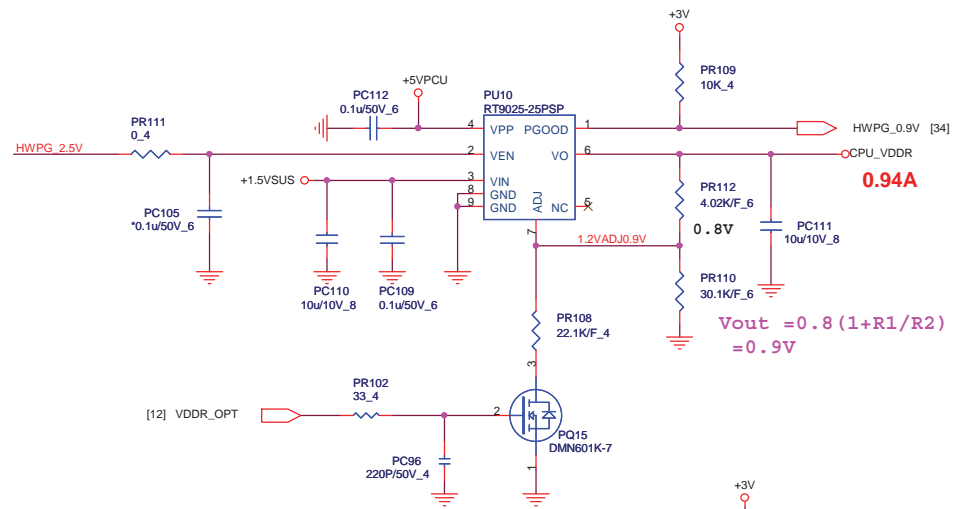
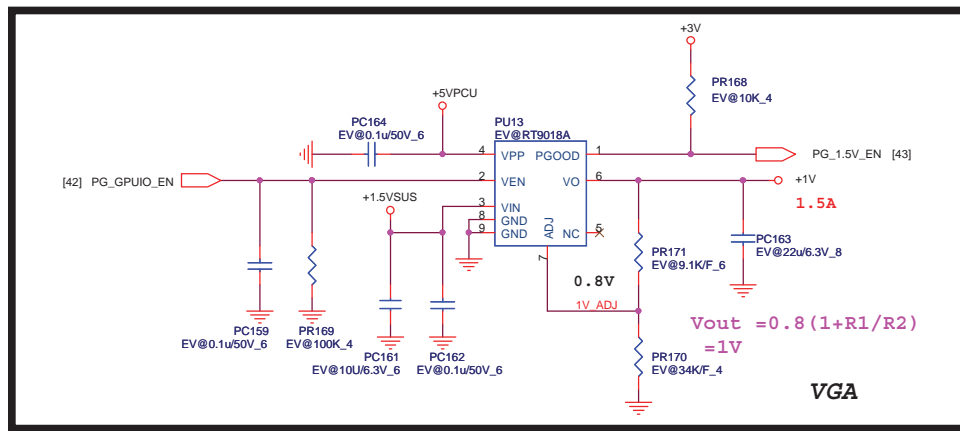



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

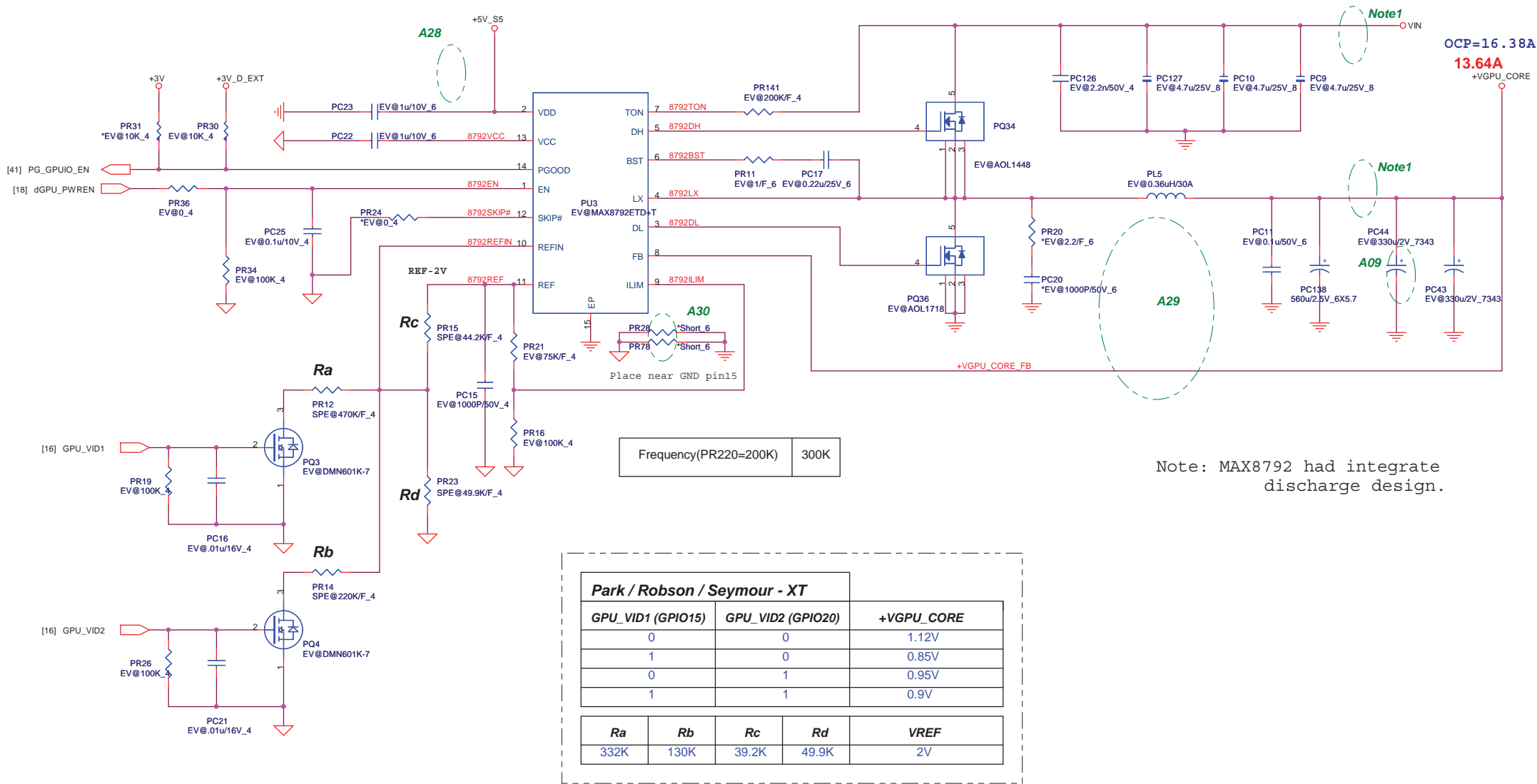


PROJECT : ZQA
Quanta Computer Inc.

Size: Document Number
DDR 1.5V(TPS51116)
 Date: Monday, May 31, 2010 Sheet 40 of 48

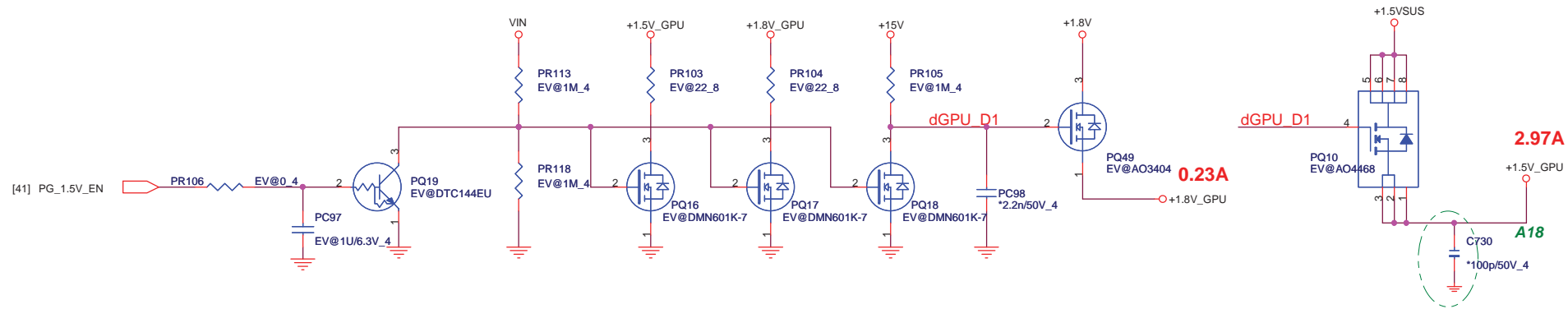



 PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number	Rev
	LDO	1A
Date:	Monday, May 31, 2010	Sheet 41 of 48



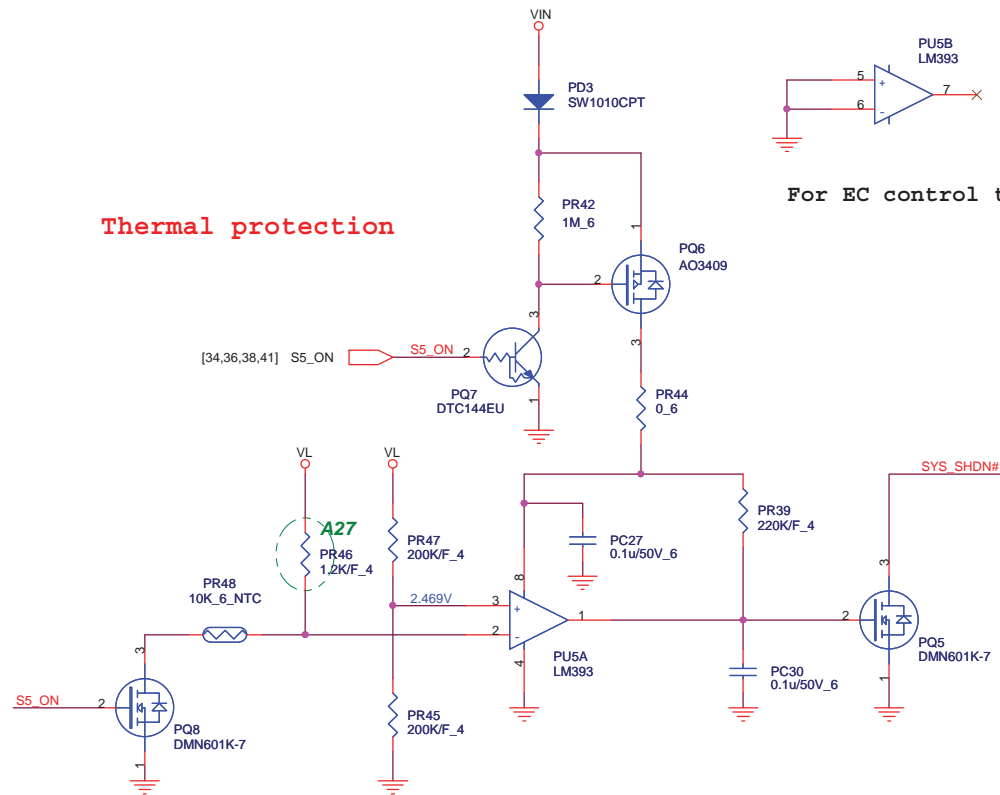
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number GPU CORE(MAX8792)	Rev 1A
Date:	Monday, May 31, 2010	Sheet 42 of 48

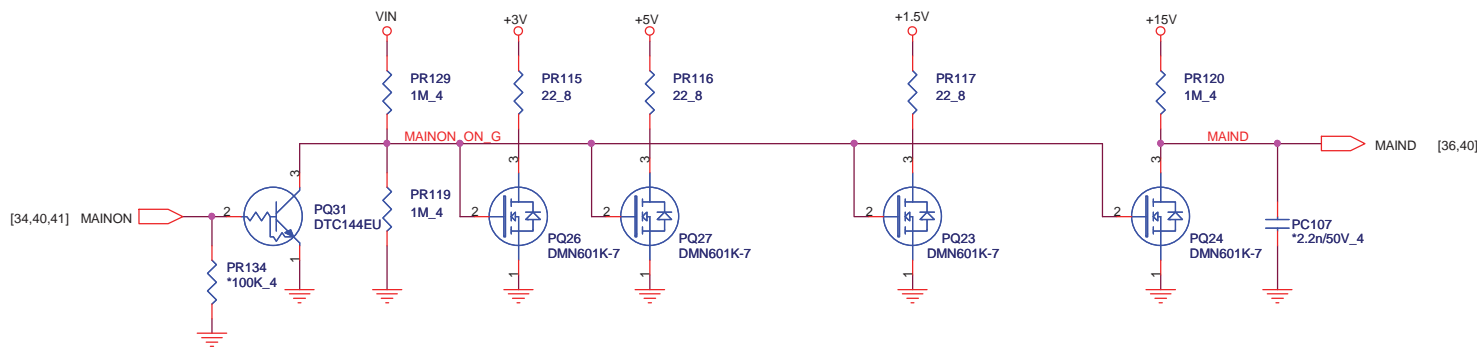
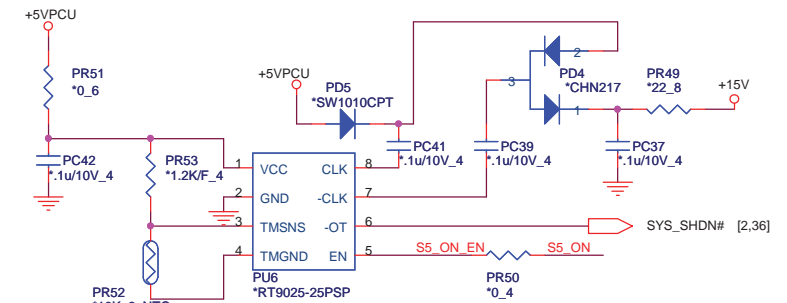


 PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number GPU POWER	Rev 1A
Date:	Monday, May 31, 2010	Sheet 43 of 48

Thermal protection

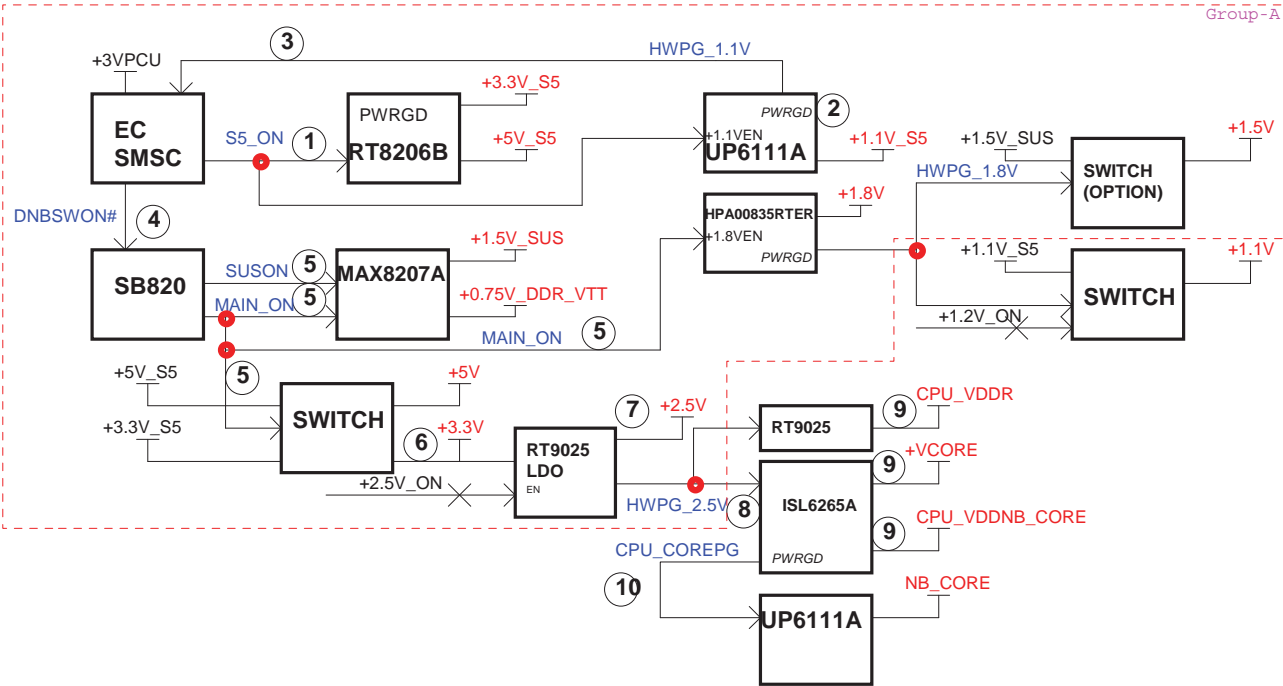


POWER TEST : Thermal & Charge pump test circuit



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	Thermal protect	1A
Date:	Monday, May 31, 2010	Sheet 44 of 48



Power on Sequence required:

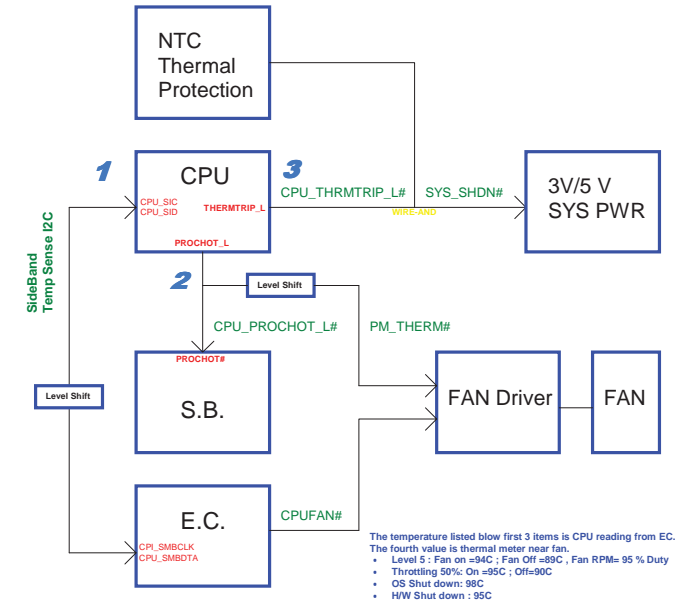
SB800:

- 1, +3.3V_S5 ramp before +1.1_S5
- 2, +3.3V ramp before +1.8v
- 3, +1.8V ramp before +1.1v
- 4, +3.3v ramp before +1.1v
- 5, +3.3VALW_R ramping down time > 300us
- 6, 50uS <= All power rails except +3.3VALW_R <= 40mS
- 7, 100uS <= +3.3VALW_R <= 40mS

RS880:

- 1, 0 < (+3.3V) - (+1.8v) < 2.1
- 2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

H/W Thermal Follow Chart



POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

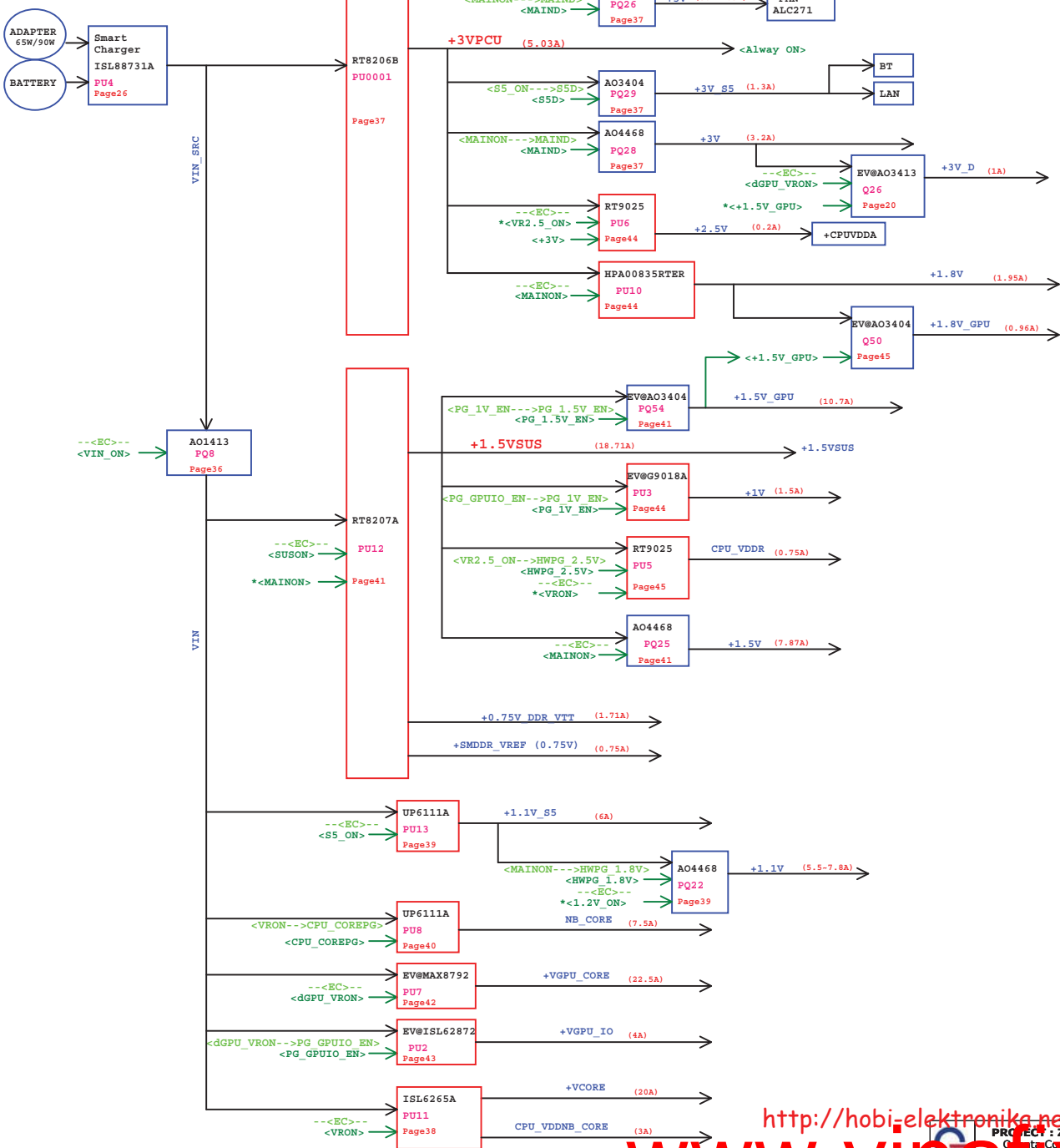
1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

PROJECT : ZQA
Quanta Computer Inc.

Size: Document Number: **PWR ON SEQ and THERM POLICY** Rev: 1A

Date: Monday, May 31, 2010 Sheet: 46 of 48

ZQ2B Power tree



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PROJECT : ZQA

Qint Computer Inc.

MODEL	REV	CHANGE LIST	Model	KN1A M/B BOARD	
			Page	From	To
ZQA M/B	3A	<p>A01 PAGE28 : Add pull high resistor 4.7kohm on PD# pin, the reason is prevent speaker no sound.</p> <p>A02 PAGE28 : Change R229,R223 to 33K for speaker 1W.</p> <p>A03 PAGE35 : Change PR8,PR142 from 1m ohm to 10m ohm.</p> <p>A04 PAGE31 : Add BT2.1 design for Customer request.</p> <p>A05 PAGE22 : Delete R8 bead.</p> <p>A06 PAGE34 : The connection of CPUFAN# is changed from 105pin to 106pin.</p> <p>A07 PAGE35 : Change P/N</p> <p>A08 PAGE35 : Change PR8 Package to 3720</p> <p>A09 PAGE42 : Stuff PC44</p> <p>A10 PAGE37 : Stuff PC165</p> <p>A11 PAGE37 : Stuff PC153</p> <p>A12 PAGE36 : Change P/N</p> <p>A13 PAGE31 : Stuff L73</p> <p>A14 PAGE31 : Stuff L45</p> <p>A15 PAGE31 : Stuff L44</p> <p>A16 PAGE31 : Add 100p for EMI</p> <p>A17 PAGE23 : Add 1000p for EMI</p> <p>A18 PAGE23 : Add 1000p for EMI</p> <p>A19 PAGE02 : Delete R356</p> <p>A20</p> <p>A21</p> <p>A22 PAGE32 : Delete EC25,EC26,EC27,EC28</p> <p>A23</p> <p>A24</p> <p>A25</p> <p>A26</p> <p>A27 PAGE44 : Change PR46 from 1.7K ohm to 1.2K ohm.</p> <p>A28</p> <p>A29</p> <p>A30</p> <p>Note :</p> <p>1. Remove Jumper : JP5,JP16,JP6,JP14,JP3,JP13,JP11,JP2,JP8,JP9,JP10,JP15,JP17,JP12,JP1,JP7</p> <p>2. Remove 0 ohm :</p> <p>R355,R356,R370,183,R207,R73,R331,L61,R76,R65,R83,R42,R50,L9,R35,R24,R27,R448,R228,R204,R202,R199,R197,R195,R223,R424,R414,R400,R442,R459,R458,R446,R62,R70,R351.</p> <p>3. Change footprint :</p> <p>C119,C139,C149,C153,C154,C181,C182,C185,C191,C192,C195,C198,C199,C201,C202,C204,C205,C209,C217,C218,C222,C224,C225,C233,C234,C235,C236,C242,C248,C249,C252,C255,C260,C261,C262,C263,C266,C268,C270,C273,C275,C277,C280,C285,C304,C307,C313,C314,C316,C318,C328,C329,C330,C332,C335,C336,C337,C338,C340,C361,C362,C363,C364,L30,L39,R9,R84,R89,R95,R96,R98,R123,R126,R134,R158,R363,C296,C308,C213</p>	1	1A	3A
			2	1A	3A
			3	1A	3A
			4	1A	3A
			5	1A	3A
			6	1A	3A
			7	1A	3A
			8	1A	3A
			9	1A	3A
			10	1A	3A
			11	1A	3A
			12	1A	3A
			13	1A	3A
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			44	1A	3A
			45	1A	3A
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			48	1A	3A
		PROJECT: ZQA	PCBA NO. http://hobi-elektronika.net	REV: 3A	DOC. NO :
		APPROVED BY : Johnny O	CHECK BY : Darren Liao	DATE: 06/11/2010	SHEET 1